

Ultra-low power, two channel capacitive sensor and touch switch for human body detection

1 General Description

The integrated circuit MS8891A is an ultra-low power, two channel capacitive sensor specially designed for human body detection. It offers two operating modes: meter mode or switch mode. In switch mode the sensor capacitance is compared with the internal reference capacitance. The sensor output changes polarity if the sensor capacitance falls below or rises above a threshold capacitance. The threshold capacitance can be individually set for both channels. The MS8891A can also be operated in meter mode where the absolute capacitance values of the sensor channels are measured. The MS8891A is configured via an I²C serial interface. The comparator outputs are available at circuit pins in switch mode or can be read via the I²C serial interface. The configuration of the various options and the operation of the meter mode are done via the I²C serial interface. After programming the configuration to the one-time-programmable (OTP) memory, the MS8891A can be operated in switch mode as a stand-alone solution.

2 Applications

- Human body detection (e.g. in-ear phone, finger detection)
- Wrist detection (e.g. wearables or medical wearables)
- Capacitive sensor
- Touch and proximity switch

3 Typical application

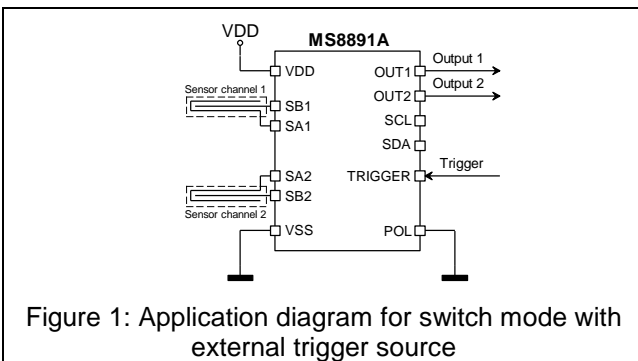


Figure 1: Application diagram for switch mode with external trigger source

4 Features

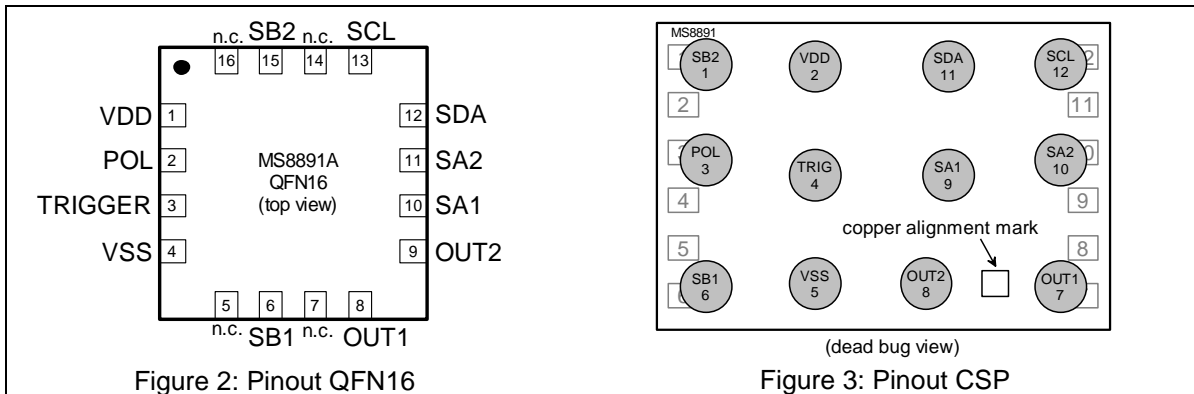
- Two capacitive sensor channels with individual outputs and inputs
- One or two channel operation
- Meter mode or switch mode
- Capacitance meter with 4 measuring ranges covering 0 to 1.6pF with a resolution of 8 bits
- Individually programmable threshold capacitance for both sensor channels in switch mode
- Programmable measuring interval in switch mode (single trigger, 2 measurements/s, 32 measurements/s, permanent)
- Programmable noise filter in switch mode
- Comparator outputs available at pins OUT1 (sensor CS1) and OUT2 (sensor CS2) in switch mode
- Polarity of comparator outputs selectable by pin POL
- OUT1 and OUT2 can be configured to output logical OR (OUT1) and AND (OUT2) combination of switch mode results
- CMOS or open-drain output drivers
- I²C serial interface available at pins SDA and SCL
- No external components needed
- Sensors capacitance can be realized with conductive tracks on PCB or casing
- Idle current typ. 50nA
- Active current during measurement typ. 11µA
- Average current for 2 measurements/s in switch mode typ. 725nA (1 channel, no noise filter)
- Voltage operating range 1.8 to 4.5V
- Temperature operating range -40 to 85°C
- Available in QFN16 3x3mm or CSP12 1.52x1.03mm

5 Ordering Information

| Typ | Package | Shipping | Article No. |
|---------|----------------------|-----------|-------------|
| MS8891A | QFN16 3x3mm | tape&reel | 9160407 |
| | CSP12 1.52x1.03mm | tape&reel | 9160406 |

Table 1: Ordering information

6 Pinout



7 Pin description

| Pin QFN | Pin CSP | Symbol | Type | Description |
|---------|---------|---------|----------------|--|
| 1 | 2 | VDD | supply | Positive supply voltage |
| 2 | 3 | POL | digital input | Sets polarity of OUT1 and OUT2 POL = '0': OUTx is high if $C_{\text{sensor}} < C_{\text{TH}}$ POL = '1': OUTx is high if $C_{\text{sensor}} > C_{\text{TH}}$ |
| 3 | 4 | TRIGGER | digital input | External trigger to start measurement in switch mode. TRIGGER is also used for applying the programming voltage during programming of the OTP memory. |
| 4 | 5 | VSS | supply | Negative supply voltage |
| 5 | | n.c. | | Not connected; pin can be left open circuit |
| 6 | 6 | SB1 | analog input | Sensor electrode, input signal sensor CS1 |
| 7 | | n.c. | | Not connected; pin can be left open circuit |
| 8 | 7 | OUT1 | digital output | Switch state output of sensor CS1 (CMOS or open-drain) |
| 9 | 8 | OUT2 | digital output | Switch state output of sensor CS2 (CMOS or open-drain) |
| 10 | 9 | SA1 | digital output | Sensor electrode, driver signal of sensor CS1 |
| 11 | 10 | SA2 | digital output | Sensor electrode, driver signal of sensor CS2 |
| 12 | 11 | SDA | digital I/O | I ² C-bus serial bidirectional data line; open drain |
| 13 | 12 | SCL | digital input | I ² C-bus serial clock input |
| 14 | | n.c. | | Not connected; pin can be left open circuit |
| 15 | 1 | SB2 | analog input | Sensor electrode, input signal sensor CS2 |
| 16 | | n.c. | | not connected; pin can be left open circuit |

Table 2: Pin description

Notes:

- SB1 and SB2 are internally switched to VSS over 8kΩ resistors when the measurement is inactive
- The inputs TRIGGER and POL must be connected to valid logic levels in the application

8 Description

8.1 Basic functionality

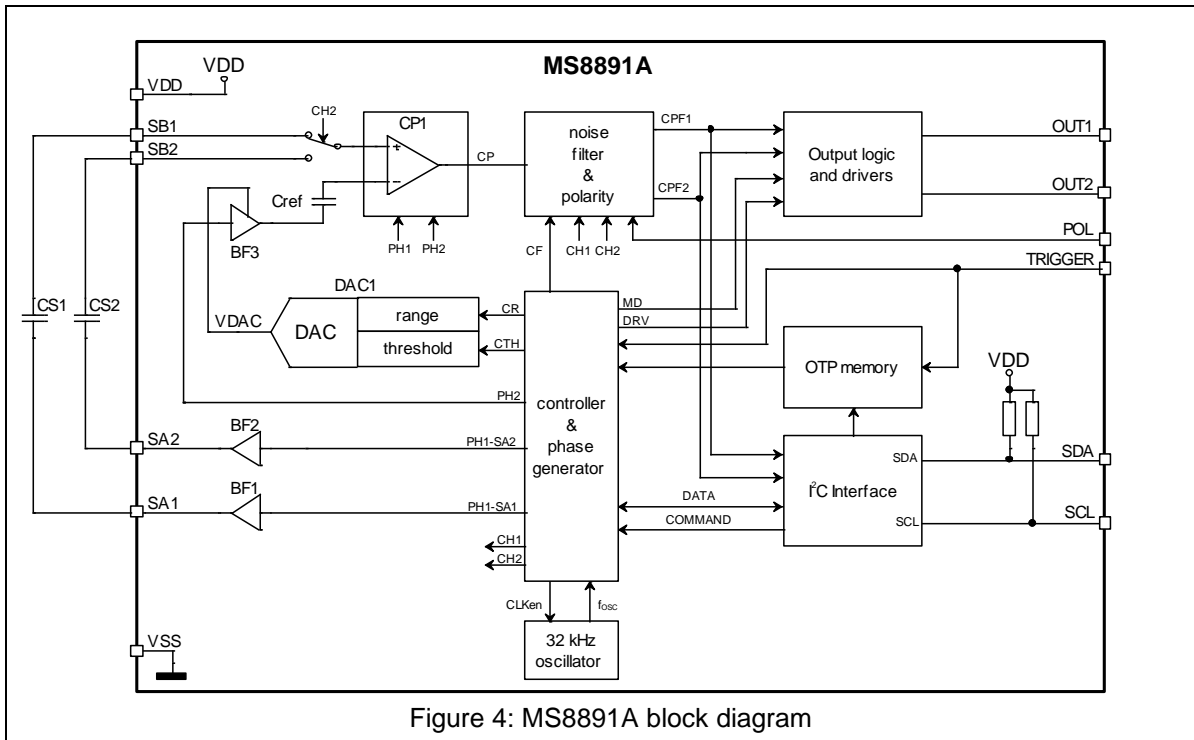


Figure 4 shows the block diagram of the circuit MS8891A. The circuit has two capacitive sensor channels CS1 and CS2. Sensor channel CS1 consists of sensor output SA1 and sensor input SB1, sensor channel CS2 of sensor output SA2 and sensor input SB2. The sensor outputs (SA1, SA2) are separated to allow independent function of the sensor channels. The sensor capacitance is measured by comparing the charge transferred at the sensor input with a reference charge defined by Cref and the voltage VDAC. VDAC is the output of the digital-to-analog converter DAC1. The equilibrium, where both charges are equal is found with a binary search. The equilibrium is defined by the following equation.

$$V_{DD} \cdot CS = VDAC \cdot Cref$$

The MS8891A can be operated in meter mode or switch mode. In meter mode, the sensor capacitances CS1 and CS2 are measured and converted to 8-bit digital values which represent the absolute sensor capacitances. The measured values are read via the I²C serial interface. In switch mode the charge transferred at the sensor input, which linearly depends on the sensor capacitance, is compared with a reference charge defined by Cref and VDAC. If the sensor capacitance drops below or rises above the threshold capacitance value (CTH1 for CS1, CTH2 for CS2) is detected by the comparator CP1 and indicated by a change of the signal CP from logical 0 to logical 1. Noise suppression is done with a programmable noise filter. The noise filter has three levels (no, low and high filter). The signals CPF1 (sensor channel 1) and CPF2 (sensor channel 2) are the sensor outputs after the noise filter and input to the output logic (direct or combinational output) with the adjacent output drivers (CMOS or open-drain). The final results are available at the outputs OUT1 and OUT2. The polarity of sensor signals CPF1 and CPF2 can be set by the input POL (POL = '0': CPFx is logical '1' if CSx is smaller than CTHx; POL = '1': CPFx is logical '1' if CSx is larger than CTHx). The input POL is evaluated during the measuring sequence and has to be stable during this time. The states of the switch mode output signals CPF1 and CPF2 can be read via the I²C serial interface. Several options can be programmed to adapt the capacitive sensor function to the application. The options are detailed in sections 8.1.7 to 8.1.10.

8.1.1 Measuring sequence in switch mode

In switch mode the capacitance at the sensor channel is compared with a threshold capacitance. This is done by comparing charges. The results of the comparison are available at the outputs OUT1 and

OUT2 or over the I²C serial interface. A measuring sequence in switch mode is either started with a single trigger (over input pin TRIGGER or by the I²C serial command COMP; only one measuring sequence is started) or executed periodically. The measuring method/interval is defined by option MI in the options register OPT1 and by the logical value of pin TRIGGER.

The measuring sequence always has the same format. It starts with the evaluation of sensor CS1 followed by the evaluation of sensor CS2. Each measuring cycle has 1 (M1), 4 (M1 to M4) or 16 (M1 to M16) measuring phases. The number of measuring phases is defined by the level of the noise filter. The level of the noise filter is set according to option CF in the options register OPT1. The noise filter is switched off completely if option NoF (options register OPT2) is set to logical '1'. The evaluation results are available after the end of the completed measuring sequence. Figure 5, Figure 6 and Figure 7 show the measuring sequences for different filter levels and for two sensor channels (CS1 and CS2). Only sensor channel CS1 is evaluated if bit SNG in the register OPT1 is set to logical '1'.

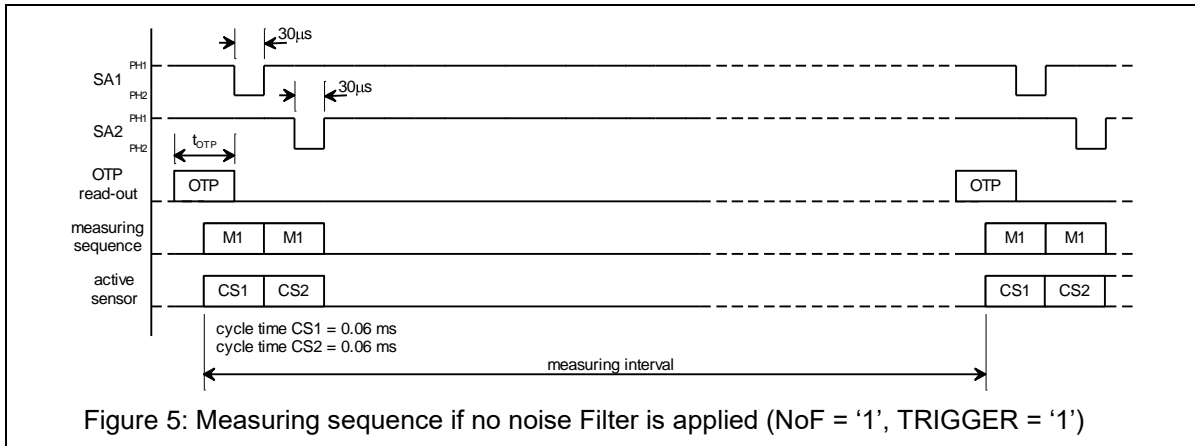


Figure 5: Measuring sequence if no noise Filter is applied (NoF = '1', TRIGGER = '1')

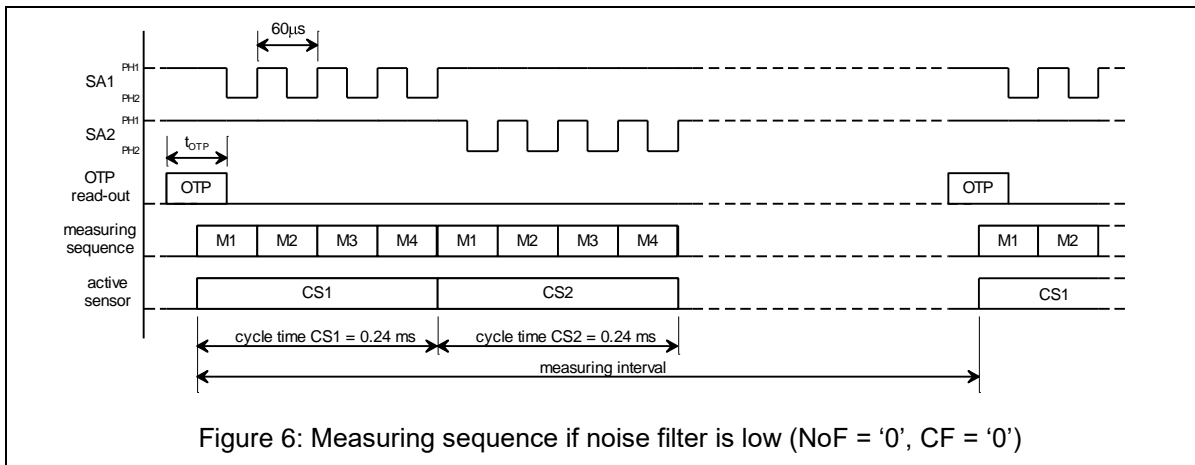


Figure 6: Measuring sequence if noise filter is low (NoF = '0', CF = '0')

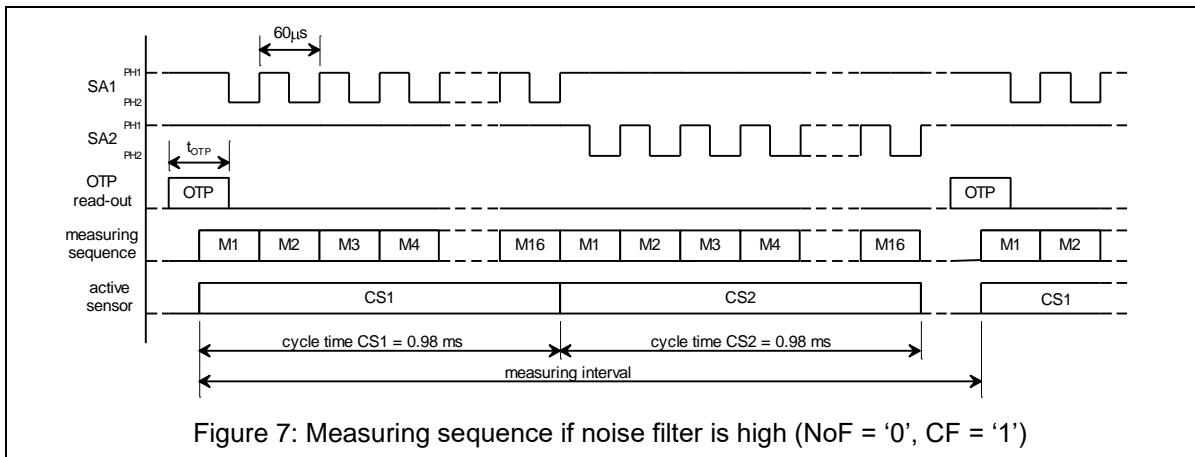


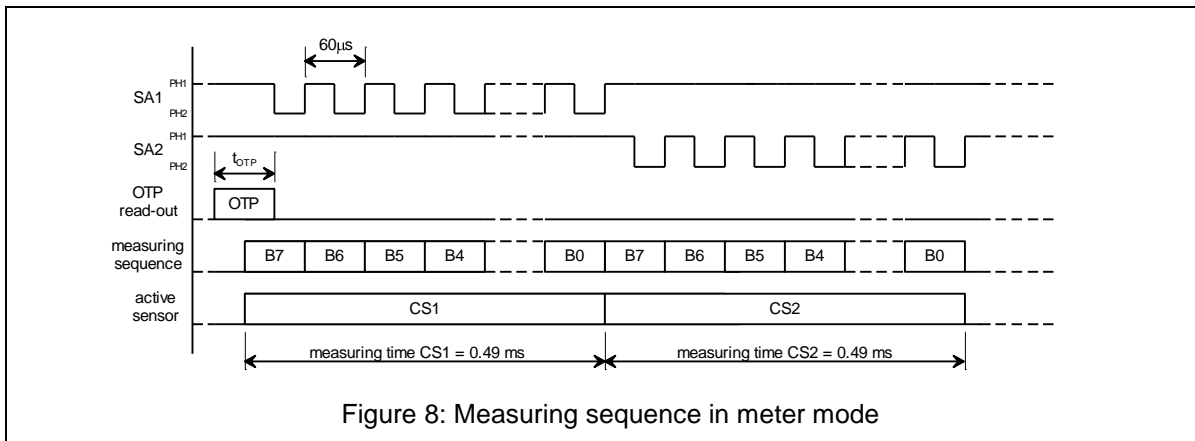
Figure 7: Measuring sequence if noise filter is high (NoF = '0', CF = '1')

The OTP memory read-out sequence is started $\frac{1}{2} t_{OTP}$ before the first measuring phase M1 and stopped at the first falling edge of SA1. The duration of t_{OTP} is equal to one measuring phase. The read-out of the OTP memory bits can be suppressed in RAM mode (register OPT2). This can be important for proper evaluation of the threshold capacitance. RAM mode is only possible if input TRIGGER is set to logical '1'.

8.1.2 Measuring sequence in meter mode

The meter mode is used to measure the absolute sensor capacitances of CS1 and CS2. The measured values of CS1 and CS2 can be used to configure the switch mode or used in a connected microcontroller for further evaluation. The meter mode is started by sending the command MCS to the MS8891A. Meter mode is only possible if input TRIGGER is set to logical '1' and the measuring interval MI in the options register OPT1 is set to single trigger before applying the command MCS. The command MCS runs through the measuring sequence as shown in Figure 8. The sensor capacitance CS1 is measured first followed by CS2. The 8-bit digital capacitance value (B7 to B0) is evaluated with a successive approximation ADC via a binary search through all quantization levels. The measurement is finished after the measurement of the last bit (B0) of CS2. The MS8891A enters the idle mode (oscillator disabled) after the end of the measurement.

Only sensor channel CS1 is measured if bit SNG in the register OPT1 is set to logical '1'.



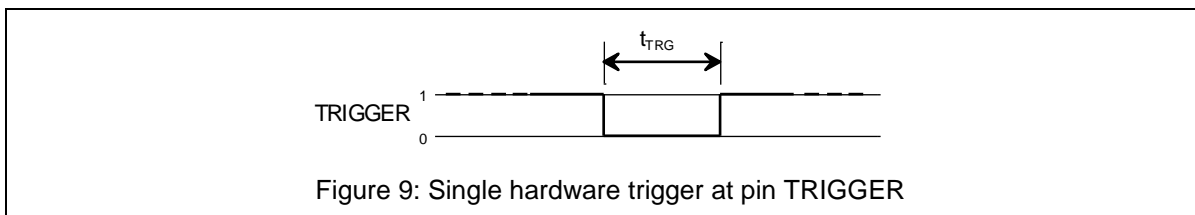
8.1.3 Clock generation and current consumption

The MS8891A contains an integrated oscillator as main clock source. The oscillator runs nominally at $f_{OSC} = 32.8\text{kHz}$. The oscillator is used to control the measuring interval and the measuring sequences and runs continuously if the measuring interval MI is set to periodic or permanent. The current consumption is highest during the measurement sequence where measurements blocks are active.

The oscillator is not needed to control the measuring interval if the measuring interval MI is set to single trigger. In this case the oscillator is switched off at the end of the measuring sequence and the MS8891A enters the idle state.

8.1.4 Single hardware trigger (switch mode)

Pin TRIGGER can be used to trigger one single compare measurement. A negative pulse at pin TRIGGER of duration t_{TRG} activates a single trigger. A single measuring sequence is started after the time t_{TRG} . A trigger of a single measurement is only possible if the measuring interval MI is set to single trigger.



8.1.5 Single software trigger (switch mode)

Command COMP executes one single compare measurement. A trigger of a single measurement is only possible if the measuring interval MI is set to single trigger and pin TRIGGER is set to logical '1'.

8.1.6 Stand-alone operation in switch mode

After programming the non-volatile memory, the MS8891A can be used in switch mode without control of a microcontroller. Pin TRIGGER must be set to logical '0' for periodic or permanent measuring interval or to logical '1' for single trigger operation.

Pin TRIGGER set to logical '0' automatically starts a compare measurement about 30ms after power-up. This first measurement reads-out the non-volatile memory and sets the programmed options. The following measurements are executed according to the programmed interval. The measuring interval is 32 measurements per second if the measuring interval MI is not programmed (MI[1:0] = '00')

Registers CTH1, CTH2 and OPT1 are always overwritten by the non-volatile memory contents prior to a measurement if pin TRIGGER is set to logical '0'. Register OPT2 is in reset state if pin TRIGGER is set to logical '0'.

8.1.7 Measuring range

Four measuring ranges can be selected according to the following table in the options register OPT1. The measuring ranges can be individually selected for CS1 (option CR1) and CS2 (option CR2).

| Range CR | ADC/DAC Resolution CU | CS range | | Unit |
|-------------|-----------------------------|----------|------|------|
| | | Min. | Max. | |
| 1 | 1.6 | 0 | 400 | fF |
| 2 | 1.6 | 400 | 800 | fF |
| 3 | 1.6 | 800 | 1200 | fF |
| 4 | 1.6 | 1200 | 1600 | fF |

Table 3: Measuring range

8.1.8 Noise filter

The output CP of the comparator is input to a digital noise filter. Three different levels of noise suppression can be selected:

- No noise filter
The noise filter is switched-off if option NoF in the options register OPT2 is set. Option NoF overrules the settings made with option bit CF. The noise filter can only be disabled with option bit NoF if pin TRIGGER is set to logical '1'.
- Noise suppression CF = low
4 measurements are performed per measurement cycle. The signal at the output of the noise filter (CPF1 or CPF2) changes the state if at least 3 measurements per measurement cycle are equal (= 3 detections). The signal at the output of the noise filter remains at its previous state otherwise.
- Noise suppression CF = high
16 measurements are performed per measurement cycle. The signal at the output of the noise filter (CPF1 or CPF2) changes the state if at least 12 measurements per measurement cycle are equal (= 12 detections). The signal at the output of the noise filter remains at its previous state otherwise.

| Noise suppression | NoF | CF | Measurements per sensor | Minimum number of detections | Measuring sequence | |
|-------------------|-----|----|-------------------------|------------------------------|--------------------|----------|
| | | | | | 2 sensors | 1 sensor |
| No | 1 | x | 1 | 1 | 0.12 ms | 0.06 ms |
| Low | 0 | 0 | 4 | 3 | 0.49 ms | 0.24 ms |
| High | 0 | 1 | 16 | 12 | 1.95 ms | 0.98 ms |

Table 4: Noise suppression

Note: The measuring sequence time does not include the OTP read-out time (see section 8.1.1).

8.1.9 Hysteresis

The comparator has a built-in hysteresis as an additional noise filter. The amplitude of the hysteresis is equal to +/- CU. CU is the unit capacitance and typically 1.6fF. The hysteresis is switched off in meter mode and is also switched off when the noise filter is switched off (bit NoF in options register OPT2).

8.1.10 Measuring interval

In switch mode the measuring sequence can be executed once (single trigger), periodically or permanently. Four options are available. The minimum measurement interval is given by twice the time of the measurement sequence plus 1/2 t_{OTP}.

| Noise suppression CF | Measuring interval MI | | | | |
|----------------------|-----------------------|---------------------------|----------------------------|---------------------------------|----------|
| | single trigger | periodic slow | periodic fast | Permanent (measuring frequency) | |
| | | | | 2 sensors | 1 sensor |
| No | single measurement | 2 measurements per second | 32 measurements per second | 3.6 kHz | 6.6 kHz |
| Low | | | | 1.0 kHz | 1.9 kHz |
| High | | | | 0.25 kHz | 0.5 kHz |

Table 5: Measuring interval

8.1.11 Output logic and drivers

CPF1 (sensor channel 1) and CPF2 (sensor channel 2) are outputs of the digital noise filter and input to the output logic with the adjacent output drivers. The truth table of the output logic is given in Table 6. Option bit MD (register OPT2) and input pin POL are control inputs of the combinational logic.

| MD | POL | OUT1 | OUT2 |
|----|-----|--------------------------|---------------------------|
| 0 | 0 | CPF1 | CPF2 |
| 0 | 1 | NOT CPF1 | NOT CPF2 |
| 1 | 0 | CPF1 OR CPF2 | CPF1 AND CPF2 |
| 1 | 1 | (NOT CPF1) OR (NOT CPF2) | (NOT CPF1) AND (NOT CPF2) |

Table 6: Output logic

Notes:

1. Input pin POL is only evaluated during the measuring sequence
2. Option bit MD is continuously evaluated

Option DRV (register OPT2) defines the function of the output stage. The output stage can be CMOS (output is active low or active high) or open-drain (output is active low only; high level must be externally driven).

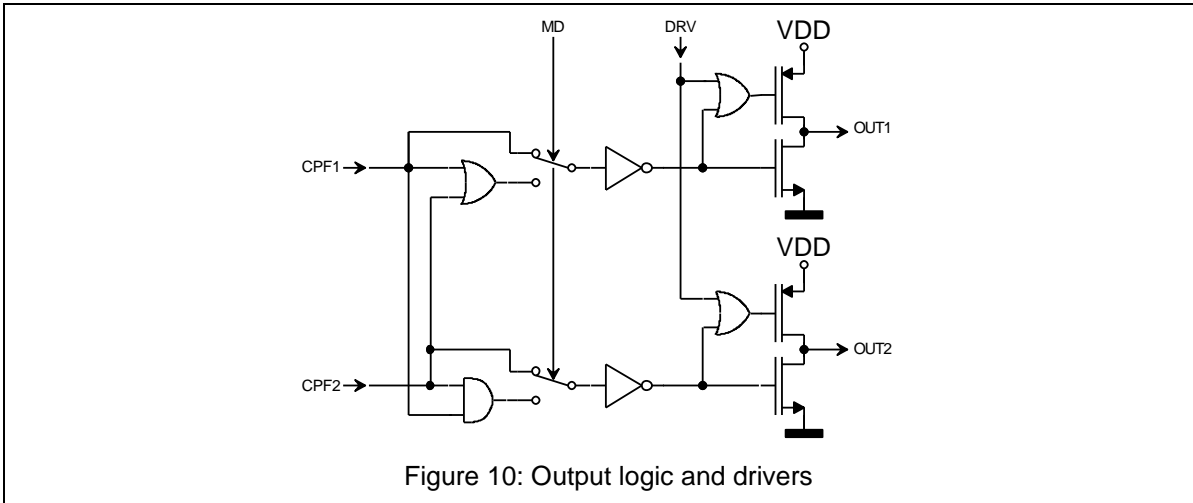


Figure 10: Output logic and drivers

9 I²C interface

The MS8891A has a slave receiver/transmitter I²C serial interface. SDA is data I/O and SCL is clock. SDA is used as an input or as an open-drain output. It is actively pulled low and is passively held high by the pull-up resistor on the I²C bus. 175kΩ Pull-up resistors are internally connected to SDA and SCL. The impedance on the I²C bus can be lowered by additional external resistors if needed.

9.1 Supported I²C protocol

The following symbol set is used in the subsequent figures showing the I²C protocol.

- **S** = START symbol
- **Sr** = START repeated
- **P** = STOP symbol
- **A** = Acknowledge bit
- = sent from I²C slave
- = sent from I²C master

9.1.1 Addressing

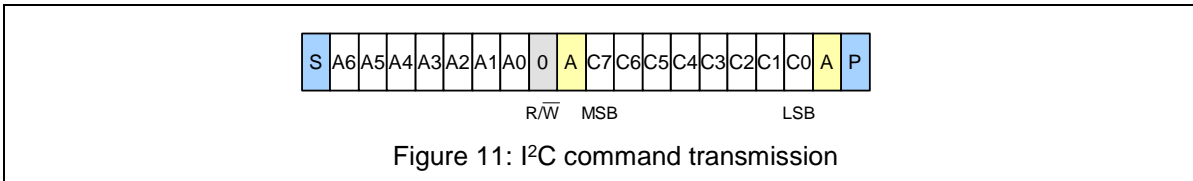
The I²C slave address has 7 bits. The fixed slave address of the MS8891A is shown in the following table.

| Bit | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|-------|----|----|----|----|----|----|----|
| Value | 0 | 1 | 0 | 0 | 0 | 1 | 0 |

Table 7: Fixed I²C slave address of MS8891A

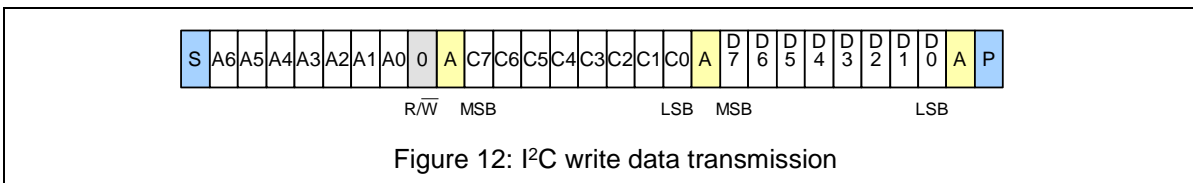
9.1.2 I²C master writes command

This protocol is used, if the I²C master only needs to send a single command to the MS8891A without additional data. The 8-bit command C7 to C0 is transmitted in the first data byte.



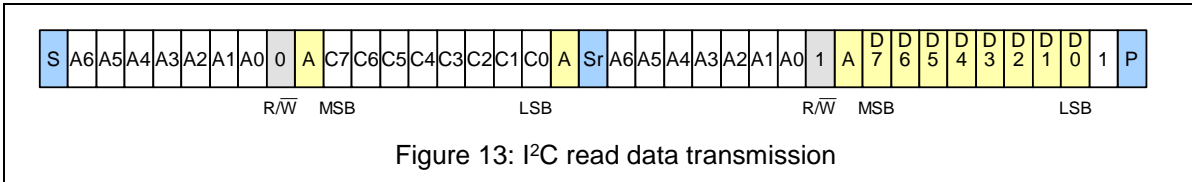
9.1.3 I²C master writes one byte

This protocol is used, when the I²C master needs to program a register. The command part (C7 to C0) specifies the write register command including the selection of the register. The data byte (D7 to D0) contains the register content to be written.



9.1.4 I²C master reads one byte

In order to read a register, the I²C master first has to send the corresponding read command. Therefore, the transmission starts with a command-write sequence. The transmission is not stopped after this. A repeated start is sent followed by a retransmission of the address. In this second part the R/W bit is set to logical high, indicating to the slave that it must transmit the data byte.



9.2 I²C command table

Table 8 is a list of all allowed commands. Other commands are not allowed.

| Command byte (C7 to C0) | Symbol | Function | Transfer type |
|-------------------------|--------|--|---------------|
| 00h | MCS | Measure CS1 and CS2 | Command |
| 01h | RCS1 | Read CS1 (register REG1) | Read 1 byte |
| 02h | RCS2 | Read CS2 (register REG2) | Read 1 byte |
| 03h | COMP | Compare (switch mode) | Command |
| 04h | RRES | Read comparison results (register RES) | Read 1 byte |
| 05h | WTH1 | Write register CTH1 | Write 1 byte |
| 06h | RTH1 | Read register CTH1 | Read 1 byte |
| 07h | WTH2 | Write register CTH2 | Write 1 byte |
| 08h | RTH2 | Read register CTH2 | Read 1 byte |
| 09h | WOPT1 | Write register OPT1 | Write 1 byte |
| 0Ah | ROPT1 | Read register OPT1 | Read 1 byte |
| 0Bh | WOPT2 | Write register OPT2 | Write 1 byte |
| 0Ch | ROPT2 | Read register OPT2 | Read 1 byte |
| 0Dh | PTH1 | Program register CTH1 to OTP memory | Command |
| 0Eh | PTH2 | Program register CTH2 to OTP memory | Command |
| 0Fh | POPT1 | Program register OPT1 to OTP memory | Command |

Table 8: I²C command table

9.3 Register description

9.3.1 Register

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset value | |
|------|-----------|---------|-------|----------|----------|-------|-------|-------|-------------|-------------|
| REG1 | REG1[7:0] | | | | | | | | '0000 0000' | |
| REG2 | REG2[7:0] | | | | | | | | '0000 0000' | |
| CTH1 | CTH1[7:0] | | | | | | | | '0000 0000' | |
| CTH2 | CTH2[7:0] | | | | | | | | '0000 0000' | |
| OPT1 | SNG | MI[1:0] | CF | CR2[1:0] | CR1[1:0] | | | | '0000 0000' | |
| OPT2 | n/a | MD | DRV | NoF | INT | RAM | | | 'xx00 0000' | |
| RES | n/a | | | | | CPF2 | CPF1 | | | 'xxxx xx00' |

Table 9: Registers

9.3.2 REG1: Capacitance value of sensor CS1

| Bit(s) | Symbol | Function | Reset value |
|--------|-----------|--|-------------|
| 7:0 | REG1[7:0] | Capacitance value of sensor CS1. The value is binary coded. The LSB value is defined by the unit capacitance CU (typ. 1.6fF) | '0000 0000' |

Table 10: Description of REG1 – capacitance value of sensor CS1

9.3.3 REG2: Capacitance value of sensor CS2

| Bit(s) | Symbol | Function | Reset value |
|--------|-----------|--|-------------|
| 7:0 | REG2[7:0] | Capacitance value of sensor CS2. The value is binary coded. The LSB value is defined by the unit capacitor CU (typ. 1.6fF) | '0000 0000' |

Table 11: Description of REG2 – capacitance value of sensor CS2

9.3.4 CTH1: Threshold capacitance for sensor CS1

| Bit(s) | Symbol | Function | Reset value |
|--------|-----------|--|-------------|
| 7:0 | CTH1[7:0] | Threshold capacitance value for sensor CS1 in switch mode. The value is binary coded. The LSB value is defined by the unit capacitor CU (typ. 1.6fF) | '0000 0000' |

Table 12: Description of CTH1 – Threshold capacitance for sensor CS1

9.3.5 CTH2: Threshold capacitance for sensor CS2

| Bit(s) | Symbol | Function | Reset value |
|--------|-----------|--|-------------|
| 7:0 | CTH2[7:0] | Threshold capacitance value for sensor CS2 in switch mode. The value is binary coded. The LSB value is defined by the unit capacitor CU (typ. 1.6fF) | '0000 0000' |

Table 13: Description of CTH2 – Threshold capacitance for sensor CS2

9.3.6 OPT1: Options register 1

| Bit(s) | Symbol | Value | Function | Reset value |
|--------|----------|------------------------------|--|-------------|
| 7 | SNG | '0' '1' | Active sensors CS1 and CS2 CS1 | '0' |
| 6:5 | MI[1:0] | '00' '01' '10' '11' | Measuring interval single trigger periodic, 32 measurements per second periodic, 2 measurements per second permanent (see Table 4 for details) | '00' |
| 4 | CF | '0' '1' | Noise suppression low (3/4 detections) high (12/16 detections) Note: Bit NoF overrules this setting | '0' |
| 3:2 | CR2[1:0] | '00' '01' '10' '11' | Measuring range CR for sensor CS2 CR = 1 CR = 2 CR = 3 CR = 4 See Table 3 for details | '00' |
| 1:0 | CR1[1:0] | '00' '01' '10' '11' | Measuring range CR for sensor CS1 CR = 1 CR = 2 CR = 3 CR = 4 See Table 3 for details | '00' |

Table 14: Description of OPT1 – options register 1

9.3.7 OPT2: Options register 2

| Bit(s) | Symbol | Value | Function | Reset value |
|--------|----------|------------------------------|---|-------------|
| 7:6 | n/a | | n/a | n/a |
| 5 | MD | '0' '1' | OUT1 = CPF1 \oplus POL; OUT2 = CPF2 \oplus POL ¹ OUT1 = (CPF1 \oplus POL) OR (CPF2 \oplus POL); OUT2 = (CPF1 \oplus POL) AND (CPF2 \oplus POL) | '0' |
| 4 | DRV | '0' '1' | CMOS output driver (OUT1, OUT2) Open-drain output driver (OUT1, OUT2) | '0' |
| 3 | NoF | '0' '1' | Noise filter switched on Noise filter switched off | '0' |
| 2:1 | INT[1:0] | '00' '01' '10' '11' | Interrupt over I ² C bus Interrupt mode disabled Interrupt if CPF1 state changes Interrupt if CPF2 state changes Interrupt if CPF1 or CPF2 state changes | '00' |
| 0 | RAM | '0' '1' | Source of configuration ROM mode: CTH1, CTH2, OPT1 are overwritten by corresponding OTP memory registers prior to measurement RAM mode: CTH1, CTH2, OPT1 are never overwritten prior to measurement | '0' |

Table 15: Description of OPT2 – options register 2

Note: The OPT2 register is in reset state if pin TRIGGER is set to logical '0'

9.3.8 RES: Comparison result register

| Bit(s) | Symbol | Value | Function | Reset value |
|--------|--------|------------|--|-------------|
| 7:2 | n/a | | n/a | n/a |
| 1 | CPF2 | '0' '1' | Comparison result sensor CS2 (CPF2) CS2 > CTH2 (POL = 0) CS2 < CTH2 (POL = 0) Note: The output value is inverted with POL = 1 | '0' |
| 0 | CPF1 | '0' '1' | Comparison result sensor CS1 (CPF1) CS1 > CTH1 (POL = 0) CS1 < CTH1 (POL = 0) Note: The output value is inverted with POL = 1 | '0' |

Table 16: Description of RES – comparison result

¹ The Boolean operator \oplus represents the “exclusive or” function

9.4 Interface timing

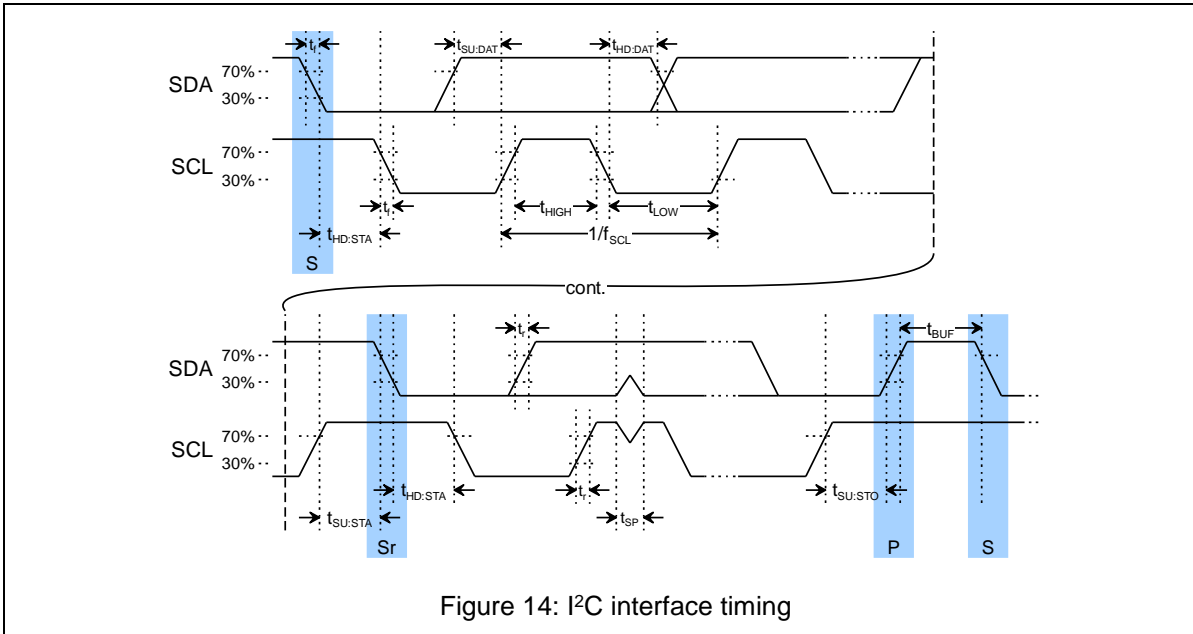


Figure 14: I²C interface timing

Note: The timing figures are specified in section 12.

9.5 Interrupt over I²C bus

In order to flag a change of the signals CPF1 or CPF2 over the I²C bus, the MS8891A can behave like an I²C master with restricted functionality. A change is signaled by sending a START condition, immediately followed by a STOP condition. This is illustrated in Figure 15. No further I²C master capabilities are supported.

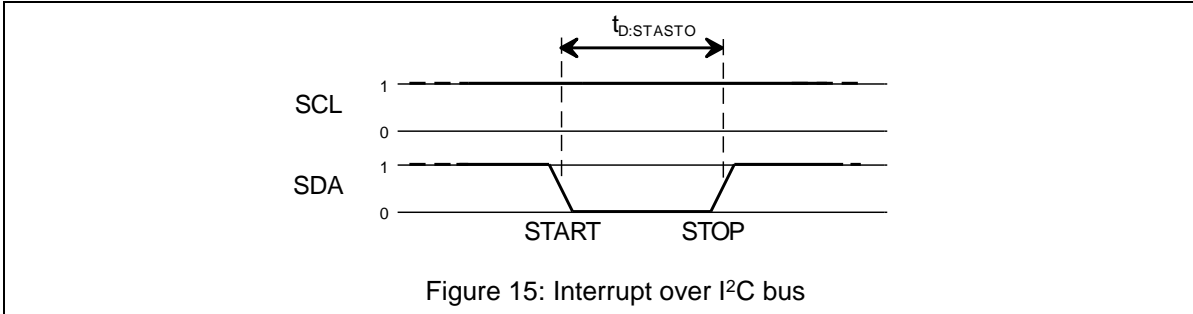


Figure 15: Interrupt over I²C bus

The I²C master has to detect the START-STOP condition and react accordingly. In order to enable this mode, the MS8891A has to be set into interrupt mode. The Interrupt mode and the interrupt conditions are specified in the register OPT2.

10 OTP memory

10.1 RAM or ROM operation

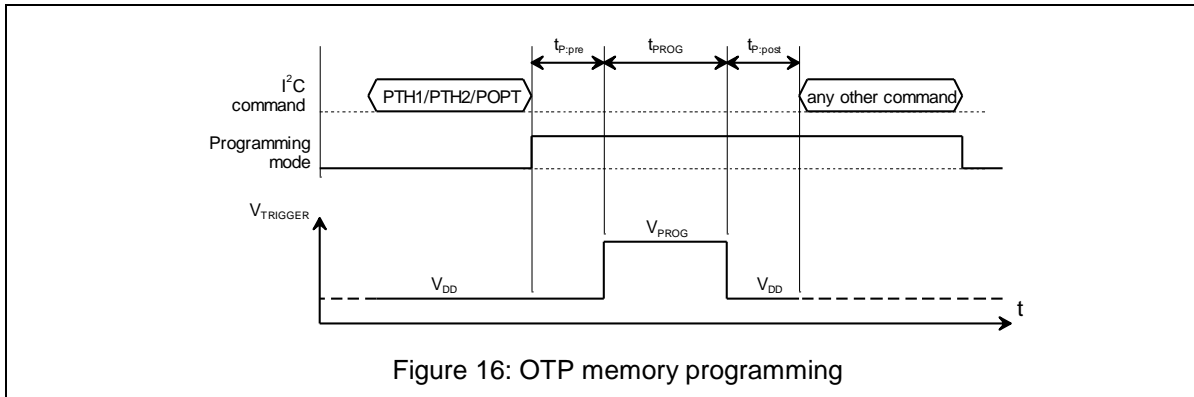
Option RAM in the register OPT2 defines if the configuration registers CTH1, CTH2 and OPT1 are overwritten by the corresponding OTP memory registers prior to each measurement. The default logical state of option RAM is '0' after power-up. This means that the registers are overwritten from the OTP memory prior to measurement. Before changing any of the registers CTH1, CTH2 or OPT1 option RAM must be set to logical '1'. This guarantees that the volatile registers CTH1, CTH2 and OPT1 are not overwritten again by the OTP memory contents prior to any measurement. Option RAM can only be set if pin TRIGGER is set to logical '1'.

10.2 OTP programming

After setting the registers CTH1, CTH2 and OPT1 the register contents can be programmed to the OTP memory. These registers must be programmed to the OTP memory if the MS8891A needs to

function stand-alone. The OTP memory bits can be programmed once from logical '0' to logical '1'. Once programmed, they cannot be reset to logical '0' anymore.

The OTP programming sequence is started with one of the commands PTH1 (OTP programming of register CTH1), PTH2 (OTP programming of register CTH2) or POPT1 (OTP programming of register OPT1). These commands enable the programming mode. The non-volatile programming of the OTP memory bits is then done by applying a programming pulse at pin TRIGGER with voltage V_{PROG} and duration t_{PROG} . The programming mode must be left latest after the OTP programming of the last register. This is done by sending any I²C command except PTH1, PTH2, POPT1 to the MS8891A.



11 Application information

11.1 Basic sensor design

Many parameters define the sensor's capacitance value and its sensitivity. It is therefore not possible to give exhaustive design guidelines. The following design guidelines are meant as a starting point for the application specific sensor design. More details are given in the MS8891A application note (separate document).

Figure 17 shows a basic sensor layout. The sensor capacitor has two electrical conductors SA (SA1 or SA2) and SB (SB1 or SB2). SA is the transmitter and SB is the receiver. The transmitter SA surrounds the receiver as much as possible. This gives the highest capacitance and also the highest immunity to noise. The sensor's capacitance is increased by increasing the sensor's antenna length l_b . The sensor's capacitance is also increased by lowering the distance d between the transmitter and the receiver and by increasing the SA and SB conductor widths w_a and w_b .

It is important to shield (e.g. with VSS lines and/or a VSS grid) the receiver antenna between the MS8891A package pins and the sensor area. The shielding capacity must not exceed 5pF. If properly shielded, the sensor is only sensitive at the sensor area and also the capacitance is only defined by the sensor area.

Figure 18 shows the typical sensor's relative capacitance value as a function of the distance to an object. The sensor capacitance is changed if an object (e.g. finger) is approaching the sensor area. The dependence between sensor capacitance and distance to the object depends on many parameters and must be evaluated in the application. A small distance d between SA and SB reduces the relative sensitivity for objects at large distances (curve A is almost flat for large distances). And a large distance d between SA and SB increases the relative sensitivity for objects at large distances (curve B is steeper than curve A for larger distances).

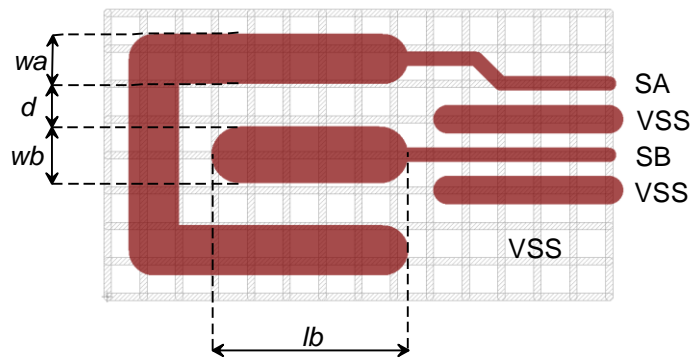


Figure 17: Basic sensor layout

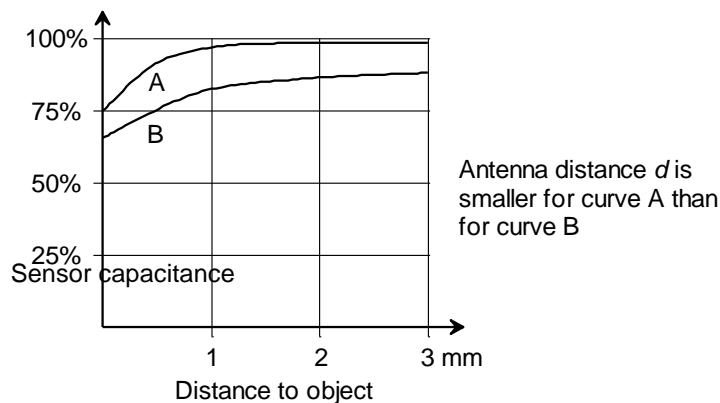


Figure 18: Sensor capacitance as a function of the distance to the object

The sensor capacitance and the relative capacitance change can be optimized with capacitance simulations of different sensor layouts.

12 Electrical Characteristics

12.1 Limiting values and ESD protection

| Name | Parameter | Min | Max | Unit |
|---------------------------------|---|------|----------------------|------|
| V _{DD} | Positive supply voltage wrt to V _{SS} | -0.5 | 9.0 | V |
| V _I | Input voltages wrt to V _{SS} | -0.5 | V _{DD} +0.5 | V |
| I _I , I _O | Input and output currents | -10 | 10 | mA |
| I _{VSS} | Total current to V _{SS} | -25 | 25 | mA |
| P _{TOT} | Power dissipation | | 100 | mW |
| T _{stg} | Storage temperature | -60 | +125 | °C |
| T _J | Junction temperature | | +125 | °C |
| V _{ESD} | Electrostatic discharge voltage (HBM JS-001-2017) | | +/- 2000 | V |

Table 17: Limiting values² and ESD protection³

12.2 DC characteristics

Conditions: V_{DD} = 3V, T_{amb} = 25°C, if not stated otherwise

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|-------------------------|--|-----|------------|-----|----------|
| V _{DD} | Positive supply voltage | | 1.8 | | 4.5 | V |
| I _{DD} | Operating current | Idle state, oscillator disabled | | 50 | | nA |
| | | Idle state, oscillator enabled, MI = periodic or permanent | | 720 | | nA |
| | | Active current during measurement CR = 1, 2 CR = 3, 4 | | 7.5 11 | | μA μA |
| | | Average current (switch mode), 2 measurements/s, NoF = '1' 2 sensors 1 sensor | | 730 725 | | nA nA |
| | | Average current (switch mode), 2 measurements/s, CF = low 2 sensors 1 sensor | | 740 735 | | nA nA |
| | | Average current (switch mode), 2 measurements/s, CF = high 2 sensors 1 sensor | | 770 750 | | nA nA |
| | | Average current (switch mode), 32 measurements/s, NoF = '1' 2 sensors 1 sensor | | 820 800 | | nA nA |
| | | Average current (switch mode), 32 measurements/s, CF = low 2 sensors 1 sensor | | 950 860 | | nA nA |
| | | Average current (switch mode), 32 measurements/s, CF = high 2 sensors 1 sensor | | 1.5 1.1 | | μA μA |
| | | Average current (switch mode), Permanent, NoF = '1' 2 sensors 1 sensor | | 12 17 | | μA μA |

² These are stress ratings only. Stress above one or more of the limiting values may cause permanent damage to the device. Operation of the device at these or at any other conditions above those given in the characteristics section of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

³ Inputs and outputs are protected against electrostatic discharge during normal handling. However, to be totally safe, it is advisable to undertake precautions appropriate to handling MOS devices.

| | | | | | | |
|---|--|--|--------------------|------|--------------------|--------------------|
| | | Average current (switch mode), Permanent, CF = low | | | | |
| | | 2 sensors | | 8 | | μA |
| | | 1 sensor | | 9.5 | | μA |
| | | Average current (switch mode), Permanent, CF = high | | | | |
| | | 2 sensors | | 6.5 | | μA |
| | | 1 sensor | | 7 | | μA |
| I_{OTP} | OTP read-out current | | | 30 | | μA |
| <i>Sensor capacitance</i> | | | | | | |
| CS_{typ} | Typical range of sensor capacitance | CR = 1 | 0 | | 400 | fF |
| | | CR = 2 | 400 | | 800 | fF |
| | | CR = 3 | 800 | | 1200 | fF |
| | | CR = 4 | 1200 | | 1600 | fF |
| CU | ADC resolution | | 1.52 | 1.6 | 1.68 | fF |
| <i>OTP memory programming characteristics</i> | | | | | | |
| V_{PROG} | OTP programming voltage | Device in OTP programming mode | 9.9 | 10.0 | 10.1 | V |
| <i>Digital inputs (MODE, SCL, SDA, SCL)</i> | | | | | | |
| V_{IL} | Input low level for digital inputs | | V_{SS} | | $0.3V_{\text{DD}}$ | V |
| V_{IH} | Input high level for digital inputs | | $0.7V_{\text{DD}}$ | | V_{DD} | V |
| <i>Digital outputs (OUT1, OUT2)</i> | | | | | | |
| V_{OL} | Output low level for digital outputs | $I_{\text{OUT}} = 2\text{mA}$ | V_{SS} | | $0.2V_{\text{DD}}$ | V |
| V_{OH} | Output high level for digital outputs | $I_{\text{OUT}} = -2\text{mA}$, DRV = '0' | $0.8V_{\text{DD}}$ | | V_{DD} | V |
| I_{OUT} | Output current | DRV = '0' | -5 | | 5 | mA |
| <i>Analog inputs (SB1, SB2)</i> | | | | | | |
| V_{AI} | | | V_{SS} | | V_{DD} | V |
| <i>I²C interface pins</i> | | | | | | |
| $V_{\text{O:SDA}}$ | Output low level on SDA | $I_{\text{SDA}} = 2\text{mA}$ | V_{SS} | | $0.2V_{\text{DD}}$ | V |
| R_{SDA} | Pull-up resistor on SDA | | | 175 | | k Ω |
| R_{SCL} | Pull-up resistor on SCL | | | 175 | | k Ω |
| <i>Temperature range</i> | | | | | | |
| T_{amb} | Operating temperature range | | -40 | 25 | 85 | $^{\circ}\text{C}$ |

Table 18: DC characteristics

12.3 AC characteristics

Conditions: $V_{DD} = 3V$, $T_{amb} = 25^{\circ}C$, if not stated otherwise

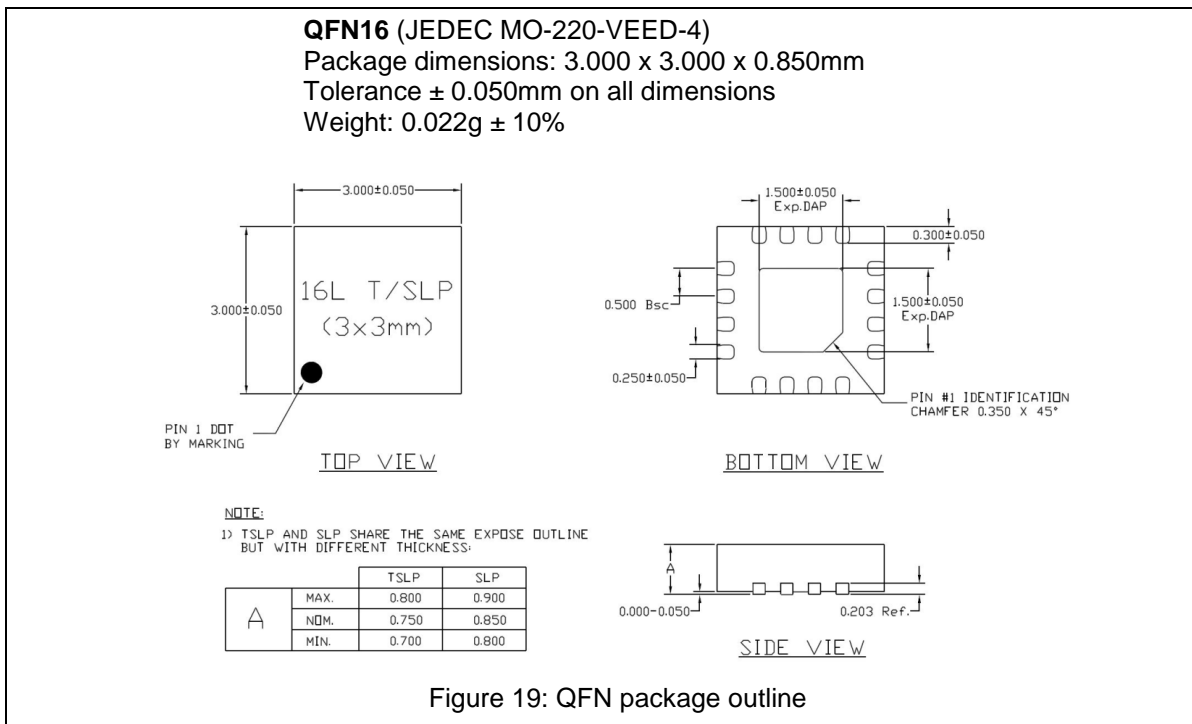
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | |
|--|--|---|-----------|------|------|------|-----|
| f _{OSC} | Oscillator frequency | MI[1:0] = '01' | 30.5 | 32.8 | 35.0 | kHz | |
| t _{meas:prox} | Measuring time for single measurement cycle in switch mode | No noise filter | | 0.06 | | ms | |
| | | CF = low | | 0.24 | | ms | |
| | | CF = high | | 0.98 | | ms | |
| t _{meas:meter} | Measuring time for single measurement sequence in meter mode | 2 sensors | | 0.98 | | ms | |
| | | 1 sensor | | 0.49 | | ms | |
| f _{MI} | Measuring frequency in switch mode | MI[1:0] = '10' | | 2 | | Hz | |
| | | MI[1:0] = '01' | | 32 | | Hz | |
| | | MI[1:0] = '11', NoF = '1' | 2 sensors | | 3.6 | | kHz |
| | | | 1 sensor | | 6.6 | | kHz |
| | | MI[1:0] = '11', CF = '0', NoF = '0' | 2 sensors | | 1.0 | | kHz |
| | | | 1 sensor | | 1.9 | | kHz |
| MI[1:0] = '11', CF = '1', NoF = '0' | 2 sensors | | 0.25 | | kHz | | |
| | 1 sensor | | 0.5 | | kHz | | |
| t _{OTP} | OTP read-out time | | | 0.06 | | ms | |
| t _{TRG} | External single trigger | | 1 | 50 | 100 | μs | |
| t _{NOF} | Delay of polarity change | Polarity change of pin TRIGGER '0' to '1' or '1' to '0' | | | 2 | ms | |
| <i>OTP programming characteristics</i> | | | | | | | |
| t _{PROG} | OTP programming pulse | | 95 | 100 | 105 | ms | |
| t _{p:pre} | Time between end of OTP programming command and start of OTP programming pulse | | 0.1 | | | ms | |
| t _{p:post} | Time between end of OTP programming pulse and start of next I ² C command | | 0.1 | | | ms | |
| <i>I²C interface characteristics (SDA, SCL)</i> | | | | | | | |
| t _{SP} | Pulse width of spikes that must be suppressed | | 0 | | 100 | ns | |
| f _{SCL} | SCL clock frequency | | 0 | | 100 | kHz | |
| t _{HD:STA} | Hold time (repeated) START condition | | 4.0 | | | μs | |
| t _{SU:STA} | Setup time (repeated) START condition | | 4.7 | | | μs | |
| t _{LOW} | LOW period of the SCL clock | | 4.7 | | | μs | |
| t _{HIGH} | HIGH period of the SCL clock | | 4.0 | | | μs | |
| t _{HD:DAT} | Data hold time | | 50 | | | μs | |
| t _{SU:DAT} | Data setup time | | 250 | | | ns | |
| t _r | Rise time SDA, SCL | | | | 1 | μs | |
| t _f | Fall time SDA, SCL | | | | 0.3 | μs | |
| t _{SU:STO} | Setup time for STOP condition | | 4.0 | | | μs | |
| t _{BUF} | Bus free time between START and STOP | | 4.7 | | | μs | |
| t _{D:STASTO} | Duration of interrupt over I ² C bus pulse on SDA line | Interrupt mode enabled | | 3 | | μs | |

Table 19: AC characteristics

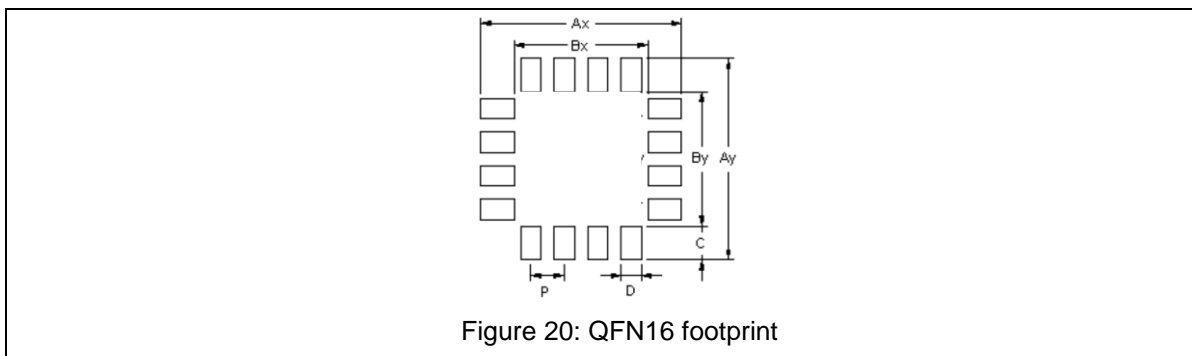
13 Production note

13.1 QFN16

13.1.1 QFN16 package outline



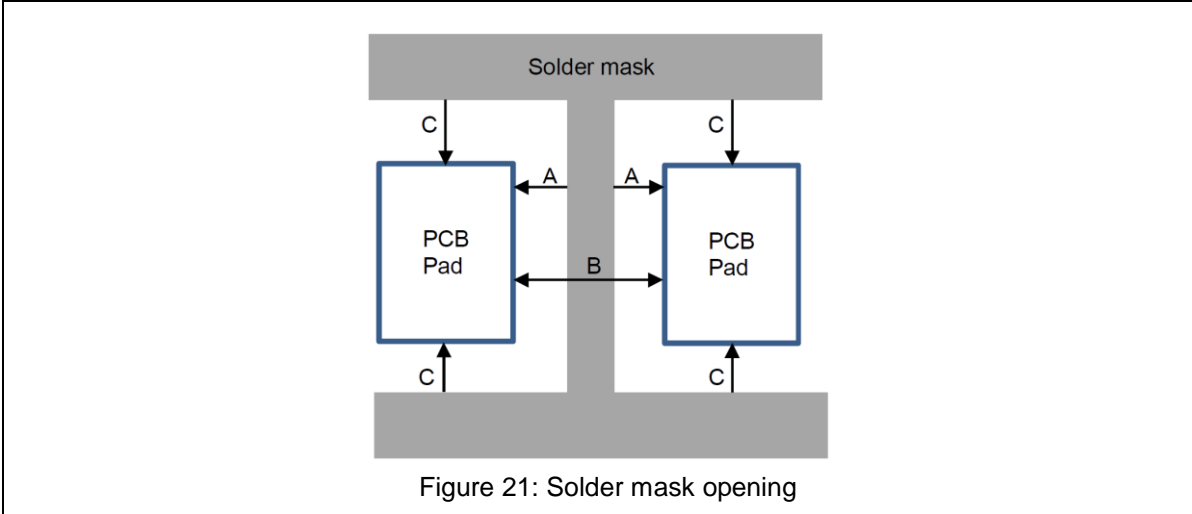
13.1.2 PCB design



| Symbol | Value | Tolerance | Unit |
|--------|-------|------------|------|
| P | 0.5 | ± 0.03 | mm |
| Ax | 3.8 | ± 0.03 | mm |
| Ay | 3.8 | ± 0.03 | mm |
| Bx | 2.1 | ± 0.03 | mm |
| By | 2.1 | ± 0.03 | mm |
| C | 0.85 | ± 0.03 | mm |
| D | 0.3 | ± 0.03 | mm |

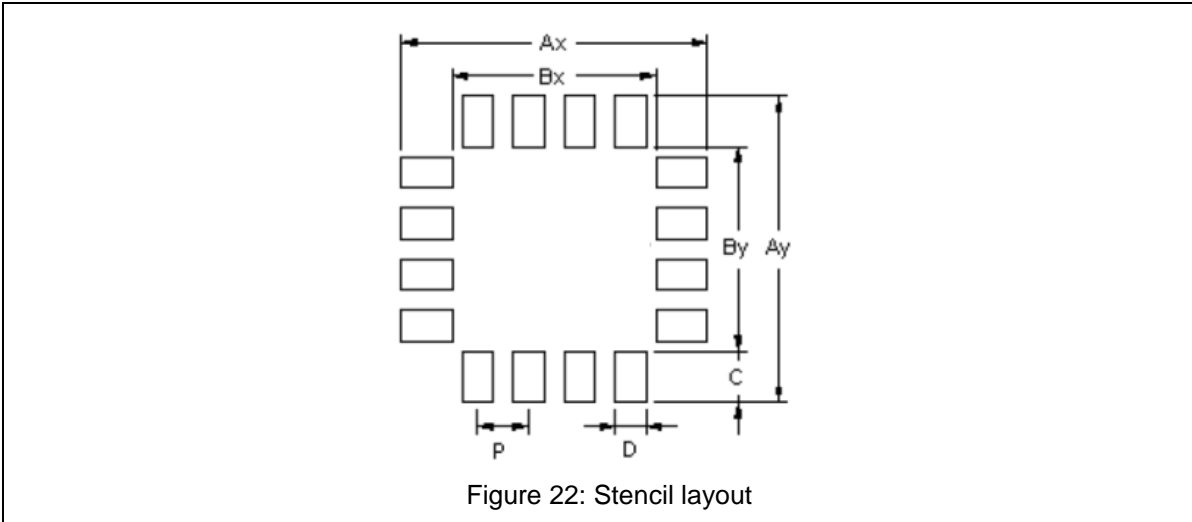
Table 20: QFN16 footprint dimensions

Solder mask opening for PCB area: If necessary, the edge of the solder mask opening around the PCB pads can be set up to the edge of the pad (A). If the distance between the pads is insufficient for the solder mask (B) then the mask can be set to the bottom and the top edges of the pads (C).



13.1.3 Assembly instructions

The recommended stencil thickness is 0.10 to 0.13mm. Refer to Figure 22 and Table 21 for layout and dimensions.



| Symbol | Value | Tolerance | Unit |
|--------|-------|-----------|------|
| P | 0.5 | ±0.03 | mm |
| Ax | 3.64 | ±0.03 | mm |
| Ay | 3.64 | ±0.03 | mm |
| Bx | 2.28 | ±0.03 | mm |
| By | 2.28 | ±0.03 | mm |
| C | 0.68 | ±0.03 | mm |
| D | 0.24 | ±0.03 | mm |

Table 21: Stencil dimensions

The recommendations in the table above are based on a stencil thickness of 0.10 to 0.13mm and the PCB footprint size given in section 13.1.2. The stencil dimensions are 80% of the footprint size. Both the stencil thickness and dimensions are recommendations. The stencil thickness and dimensions may have to be adjusted to take into account other components on the board. For example, components with leads may typically require a little more solder to compensate for co-planarity problems. Generally speaking increasing the stencil thickness and/or dimensions result in more solder being deposited and increases the risk of bridging. Decreasing the stencil thickness and/or dimensions results in less solder being deposited and increases the risk of insufficient solder for a good solder joint.

13.1.4 Recommended reflow parameters

The reflow profile is dependent on many different parameters. The profile here is given as a guide. It may be necessary to adjust the profile slightly depending on the solder flux and equipment used. The key temperature/times associated with the different reflow oven zones are defined in J-STD-020.

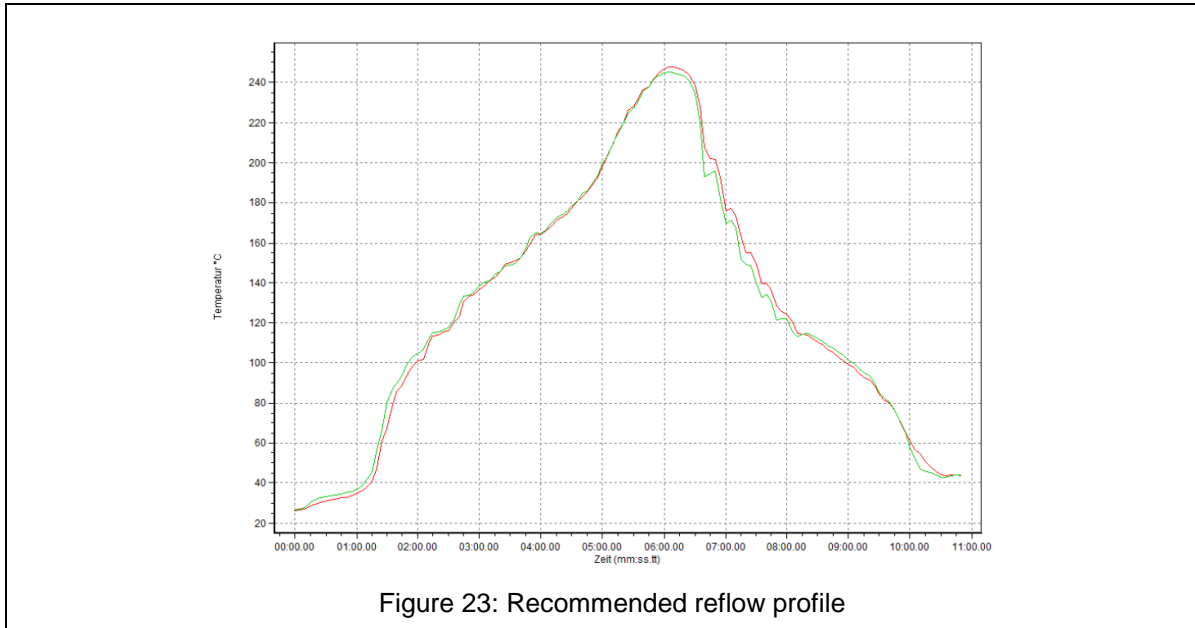
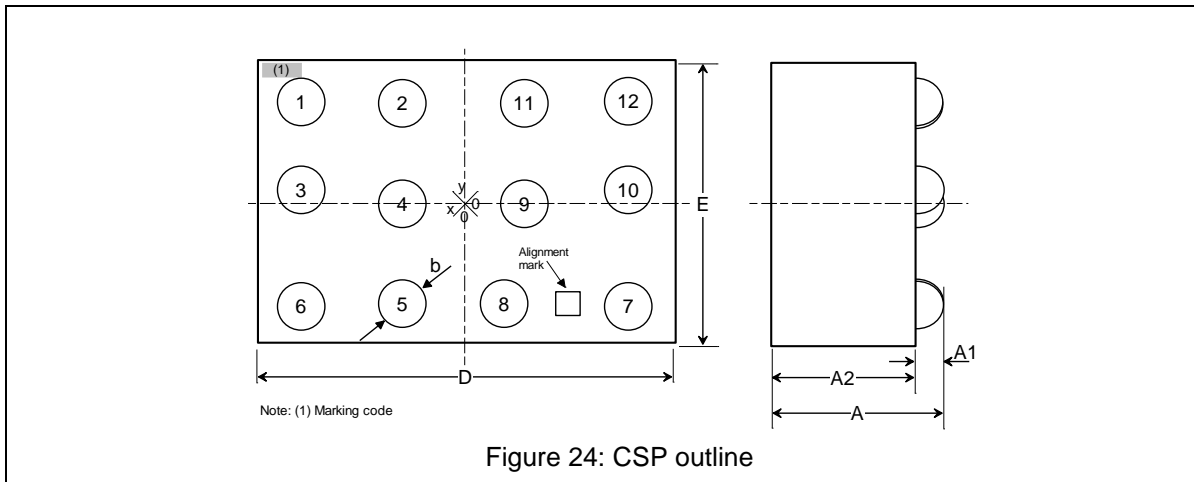


Figure 23: Recommended reflow profile

The maximum reflow temperature is 260°C. The moisture sensitivity level is 1 (MSL1).

13.2 CSP

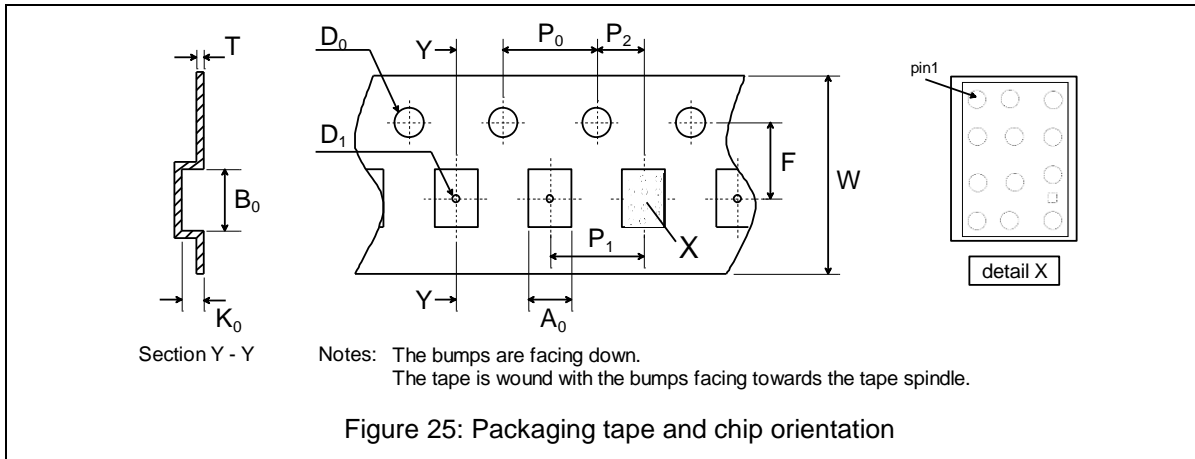
13.2.1 Bump coordinates and dimensions



| Bump No. | X (μm) | Y (μm) | Item | Value | Tolerance |
|----------------|--------|--------|---|----------------------|-----------|
| 1 (SB2) | -595 | 360 | Chip size (D) | 1.52mm | ±30μm |
| 2 (VDD) | -225 | 355 | Chip size (E) | 1.03mm | ±30μm |
| 3 (POL) | -595 | -53 | Chip thickness (A2) | 525μm | ±20μm |
| 4 (TRIGGER) | -225 | 0 | Bump height | 100μm | ±15μm |
| 5 (VSS) | -225 | -355 | Bump height inclusive redistribution (A1) | 112μm | ±19μm |
| 6 (SB1) | -595 | -362 | Chip thickness including bumps (A) | 637μm | ±39μm |
| 7 (OUT1) | 595 | -362 | Bump diameter (b) | 172μm | ±17μm |
| 8 (OUT2) | 150 | -355 | Bump placement | ±3μm | |
| 9 (SA1) | 225 | 0 | Bump material | Sn (97.5%) Ag (2.5%) | |
| 10 (SA2) | 595 | 53 | Alignment mark | 100μm x 100μm | |
| 11 (SDA) | 225 | 355 | | | |
| 12 (SCL) | 595 | 360 | | | |
| Alignment mark | 375 | -355 | | | |

Table 22: Solder bump coordinates and dimensions

13.2.2 Packaging tape

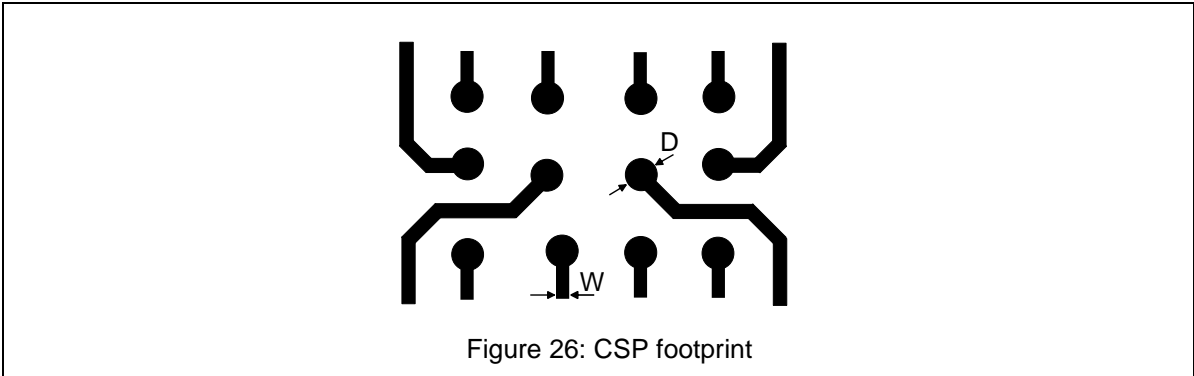


| Symbol | Description | Value | Tol. | Unit |
|----------------|---|-------|-------|------|
| A ₀ | Pocket x | 1.20 | ±0.10 | mm |
| B ₀ | Pocket y | 1.65 | ±0.10 | mm |
| D ₀ | Diameter sprocket hole | 1.55 | ±0.05 | mm |
| D ₁ | Diameter pocket hole | 0.55 | ±0.05 | mm |
| F | Center of sprocket hole to center of pocket | 3.5 | ±0.05 | mm |
| K ₀ | Pocket z | 0.7 | ±0.05 | mm |
| P ₀ | Hole pitch | 4.0 | ±0.10 | mm |
| P ₁ | Pocket pitch | 4.0 | ±0.10 | mm |
| P ₂ | Pocket to sprocket hole pitch | 2.0 | ±0.05 | mm |
| T | Tape thickness | 0.30 | ±0.05 | mm |
| W | Tape width | 8.0 | ±0.30 | mm |

Table 23: Tape dimensions for CSP package

13.2.3 PCB design

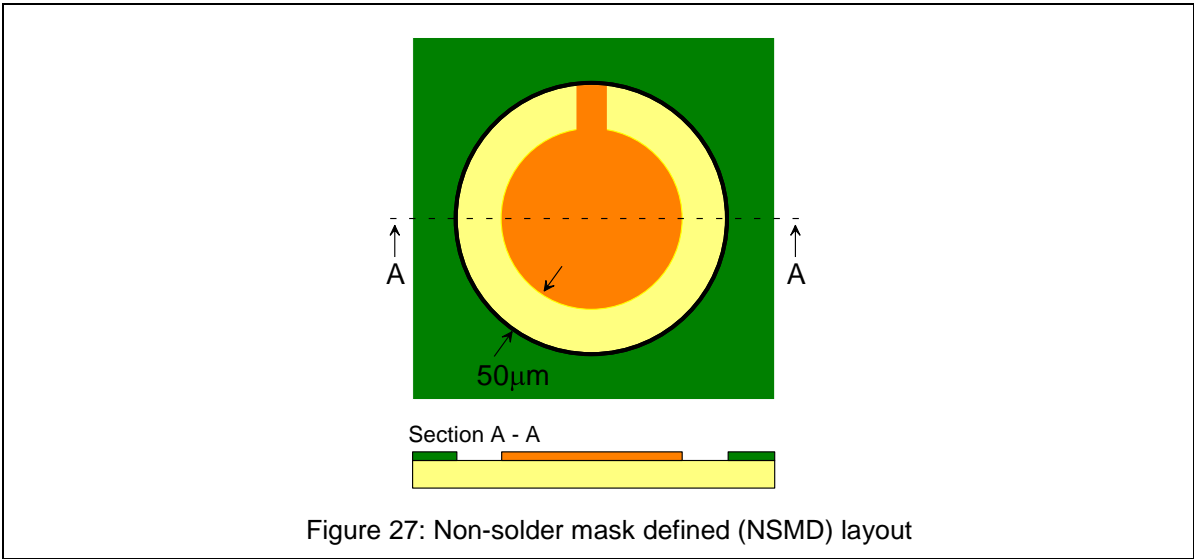
The values given in this section are recommendations for PCB designs with Ni/Au pad surface finish.



| Symbol | Description | Value | Tol. | Unit |
|--------|-------------------------|---------------|------|------|
| D | Pad diameter | 220 | ±20 | µm |
| W | Width of pad connection | 100... 200 | | µm |

Table 24: CSP footprint dimensions

It is recommended to use a non-solder mask defined (NSMD) layout for the PCB pads with a distance of 50µm between the PCB pad and the edge of the solder mask opening.



13.2.4 Assembly instructions

For solder paste deposition it is recommended to use an electropolished laser-cut stencil with a thickness of 80µm and a circular aperture with a diameter of 200µm.

It is recommended to use a type IV solder paste, preferably mildly activated (RMA), with a solder particle diameter of 20 to 38µm.

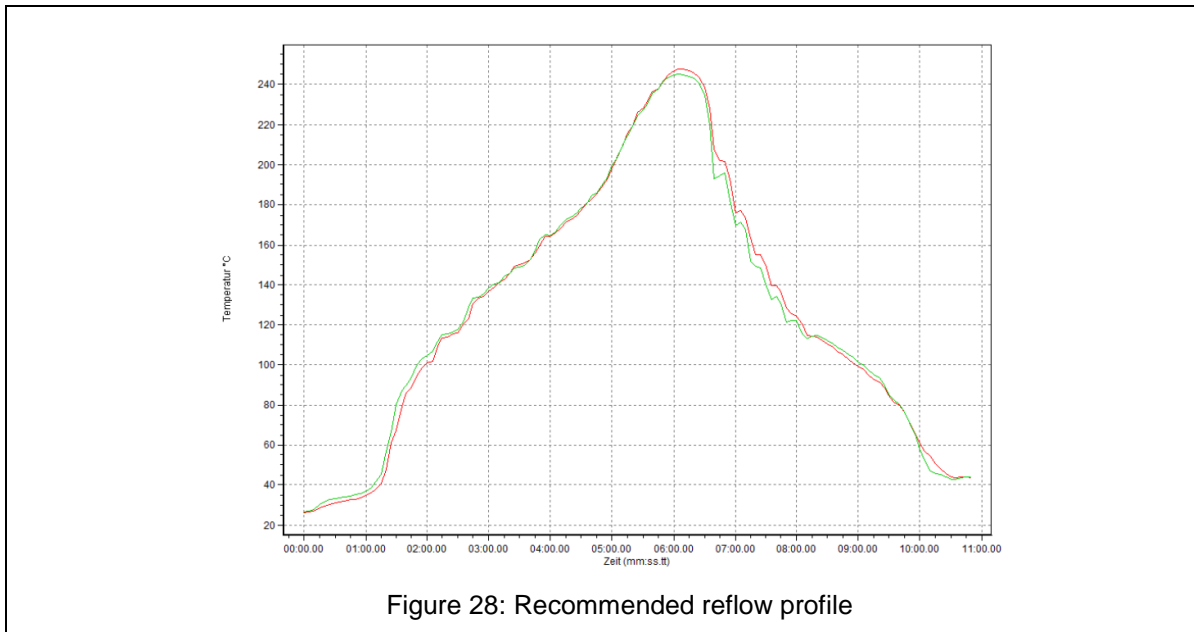
The assembly procedure for the CSP package is compatible with surface mount procedures.

The CSP package must be placed on the PCB using a pick and place machine with optical alignment. The alignment can be verified using the package outline. The misalignment must not exceed ±50µm in both directions.

The CSP package does not require underfill.

13.2.5 Recommended reflow parameters

The reflow profile is dependent on many different parameters. The profile here is given as a guide. It may be necessary to adjust the profile slightly depending on the solder flux and equipment used. The key temperature/times associated with the different reflow oven zones are defined in J-STD-020.



The maximum allowed reflow temperature is 260°C. The moisture sensitivity level is 1 (MSL1).

14 Legal disclaimer

This product is not designed for use in life support appliances or systems where malfunction of these parts can reasonably be expected to result in personal injury. Customers using or selling this product for use in such appliances do so at their own risk and agrees to defend, indemnify and hold harmless Microdul AG from all claims, expenses, liabilities, and/or damages resulting from such use of the product.

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