

## Ultra-low power capacitive sensor and touch switch for human body detection and system wake-up with absolute & relative switching threshold

**Note:** The silicon version MS8892A suffers from a design flaw, which prevents the correct operation in autonomous mode (with pin TRIGGER permanently connected to VSS level). This issue will be resolved in version MS8892B in the coming months.

### 1 General Description

The integrated circuit MS8892A is an ultra-low power capacitive sensor specially designed for human body detection and as wake-up source for ultra-low power systems. It offers two operating modes: meter mode or switch mode. In switch mode the sensor capacitance is compared with the internal reference capacitance. The capacitance threshold can be set absolutely or relative to a baseline value, which is automatically determined and therefore includes fabrication and material tolerances. The comparator output is available at a circuit pin in switch mode or can be read via the I<sup>2</sup>C serial interface. The MS8892A can also be operated in meter mode where the absolute capacitance value of the sensor is measured. The MS8892A can optionally be operated with a latching output. In this configuration it can be used as a wake-up device and directly control a power-management IC (PMIC) or a PMOS type power-switch for achieving the lowest possible power consumption for ultra-low power systems. An external clock input allows the power consumption of the MS8892A to be further minimized. This saves system power when a clock is already available from a real time clock (RTC) or nanotimer. The configuration of the various options are performed via the I<sup>2</sup>C serial interface. After programming the configuration to the one-time-programmable (OTP) memory, the MS8892A can be operated in switch mode as a stand-alone solution.

### 2 Typical application

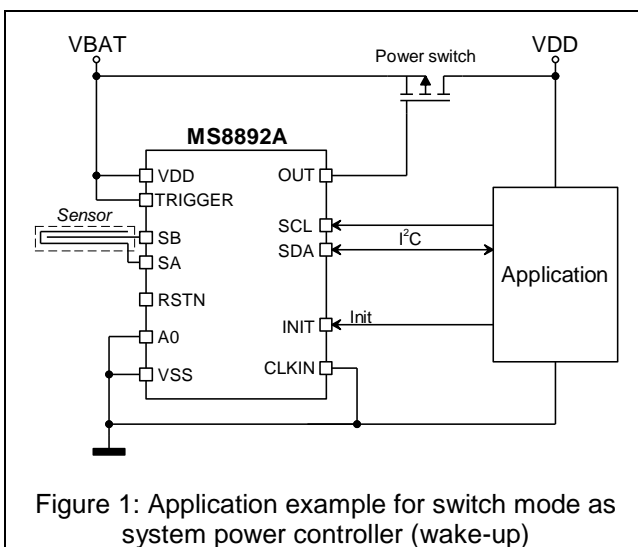


Figure 1: Application example for switch mode as system power controller (wake-up)

### 3 Applications

- Human body detection (e.g. in-ear phone, finger detection)
- Wrist detection (e.g. wearables or medical wearables)
- Capacitive sensor
- Touch and proximity switch
- System wake-up controller

### 4 Features

- Capacitive sensor with direct digital output
- Meter mode or switch mode
- Average current for 2 measurements/s in switch mode typ. 65nA (no noise filter) with external clock source
- Average current for 2 measurements/s in switch mode typ. 725nA (no noise filter)
- Idle current typ. 50nA
- Active current during measurement typ. 11µA
- Latching output to directly control power state of a PMIC or a PMOS power switch
- Capacitance meter with a measuring range covering 0.2 to 1.0pF with a resolution of 8 bits
- Individually programmable threshold capacitance in switch mode
- Automatically adjusted switching threshold in switch mode with a programmable threshold step size
- Programmable measuring interval in switch mode
- Programmable noise filter in switch mode
- Comparator output at pin OUT in switch mode
- Programmable polarity of comparator output
- CMOS or open-drain output driver
- Internal switchable pull-up resistor in open-drain configuration to avoid static current in pull-up
- I<sup>2</sup>C serial interface available at pins SDA and SCL
- I<sup>2</sup>C address pin allowing operation of two MS8892A on a single bus
- No external components needed
- Sensor capacitance can be realized with conductive tracks on PCB or casing
- Voltage operating range 1.8 to 4.5V
- Temperature operating range -40 to 85°C
- Available in QFN16 3x3x0.85mm
- Other packages possible for larger quantities

## 5 Ordering Information

Type	Package	Shipping	Article No.
MS8892A	QFN16 3x3mm	now	9160454
	CSP12 1.03x1.52mm	on request	

Table 1: Ordering information

## 6 Pinout

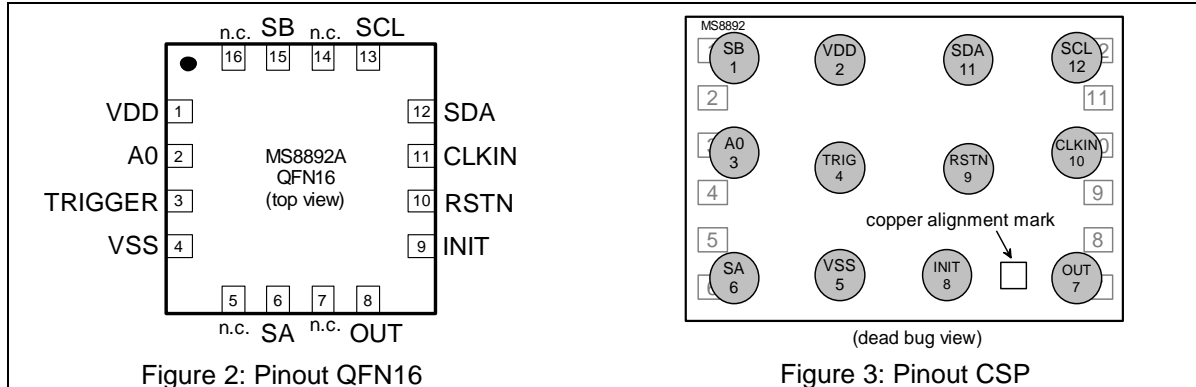


Figure 2: Pinout QFN16

Figure 3: Pinout CSP

## 7 Pin description

Pin QFN	Pin CSP	Symbol	Type	Description
1	2	VDD	supply	Positive supply voltage
2	3	A0	digital input	User-defined I <sup>2</sup> C sub-address bit 0, connect to VSS or VDD
3	4	TRIGGER	digital input	External trigger to start measurement in switch mode, connect to MCU, VDD or VSS, depending on chosen operating mode. TRIGGER is also used for applying the programming voltage during programming of the OTP memory.
4	5	VSS	supply	Negative supply voltage
5		n.c.		Not connected; pin can be left open circuit
6	6	SA	digital output	Sensor electrode, driver signal
7		n.c.		Not connected; pin can be left open circuit
8	7	OUT	digital output	Switch state output, CMOS push-pull or open-drain with integrated pull-up resistor
9	8	INIT	digital input	(Re)initialize the baseline capacitance value in relative threshold mode Resets the output state in latching mode Connect to VSS if not used in the application
10	9	RSTN	digital input	Reset input, low active, internal pull-up
11	10	CLKIN	digital input	External clock input
12	11	SDA	digital I/O	I <sup>2</sup> C-bus serial bidirectional data line; open-drain
13	12	SCL	digital input	I <sup>2</sup> C-bus serial clock input
14		n.c.		Not connected; pin can be left open circuit
15	1	SB	analog input	Sensor electrode, input signal
16		n.c.		Not connected; pin can be left open circuit

Table 2: Pin description

### Notes:

- SB is internally switched to VDD over an 8kΩ resistor when the measurement is inactive
- The inputs TRIGGER, INIT, CLKIN, A0 must be connected to valid logic levels in the application
- The input RSTN can be left floating or connected to a capacitor to VSS

**8 Description**

**8.1 Basic functionality**

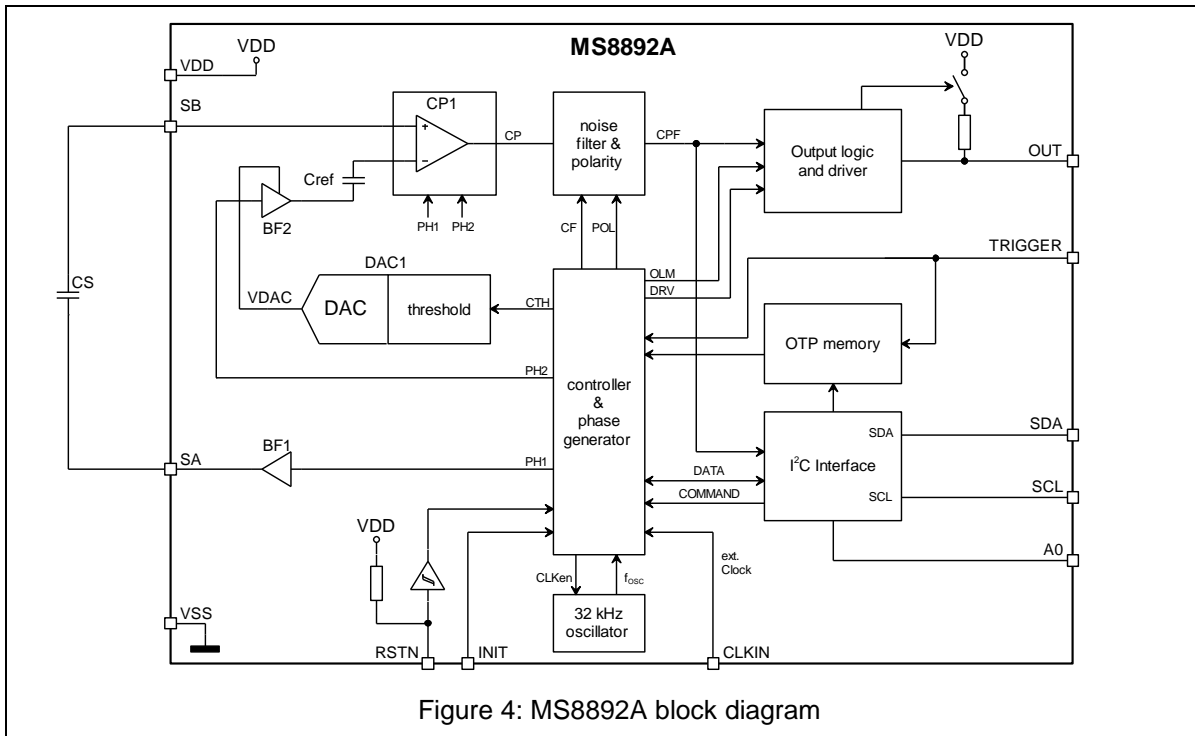


Figure 4: MS8892A block diagram

Figure 4 shows the block diagram of the circuit MS8892A. The circuit has one capacitive sensor channel CS, consisting of sensor output SA and sensor input SB. The sensor capacitance is measured by comparing the charge transferred at the sensor input with a reference charge defined by Cref and the voltage VDAC. VDAC is the output of the digital-to-analog converter DAC1. The equilibrium, where both charges are equal is defined by the following equation.

$$V_{DD} \cdot CS = VDAC \cdot Cref$$

The MS8892A can be operated in meter mode or switch mode. In meter mode, the sensor capacitance CS is measured and converted to an 8-bit digital value which represents the absolute sensor capacitance. The measured value is read out via the I<sup>2</sup>C serial interface.

In switch mode the charge transferred from SA to the SB sensor input, which linearly depends on the sensor capacitance, is compared with a reference charge defined by Cref and VDAC. If the sensor capacitance drops below or rises above the threshold capacitance value C<sub>TH</sub> is detected by the comparator CP1 and indicated by a change of the signal CP from logical '0' to logical '1'. Noise suppression is done with a programmable noise filter. The noise filter has three levels (no, low and high filter). The signal CPF is the sensor output after the noise filter and is available at the output OUT. The polarity of the sensor output can be set by the bit POL in register OPT2:

- POL = '0': OUT is logical '1' if C<sub>s</sub> is smaller than C<sub>TH</sub>
- POL = '1': OUT is logical '1' if C<sub>s</sub> is larger than C<sub>TH</sub>

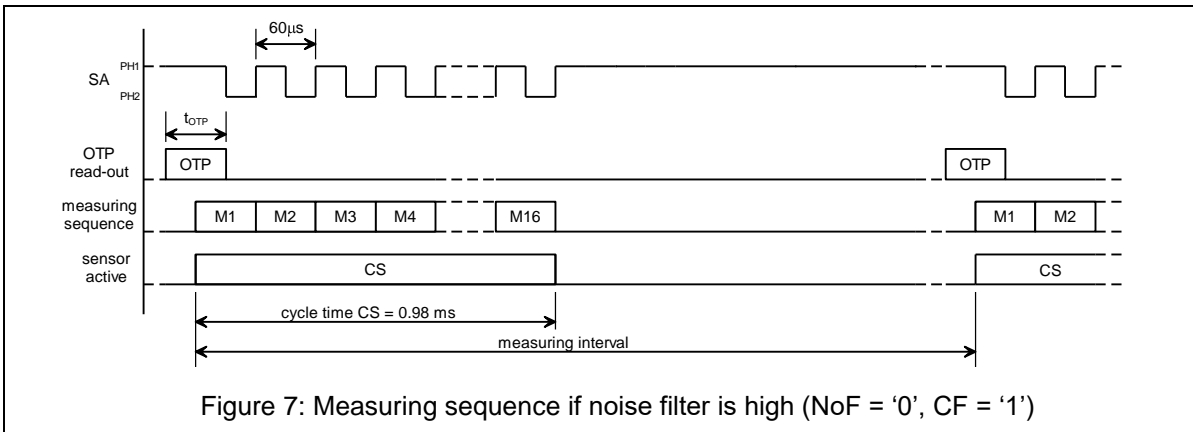
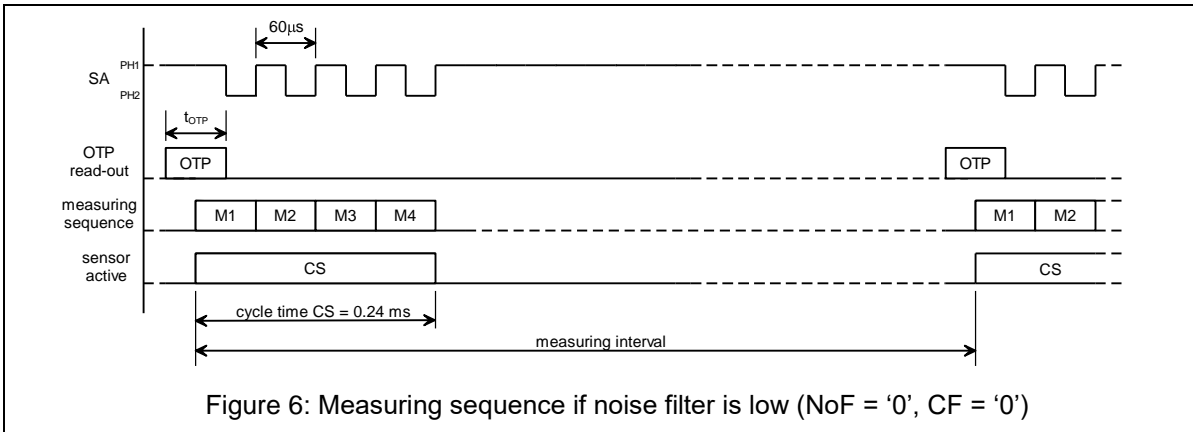
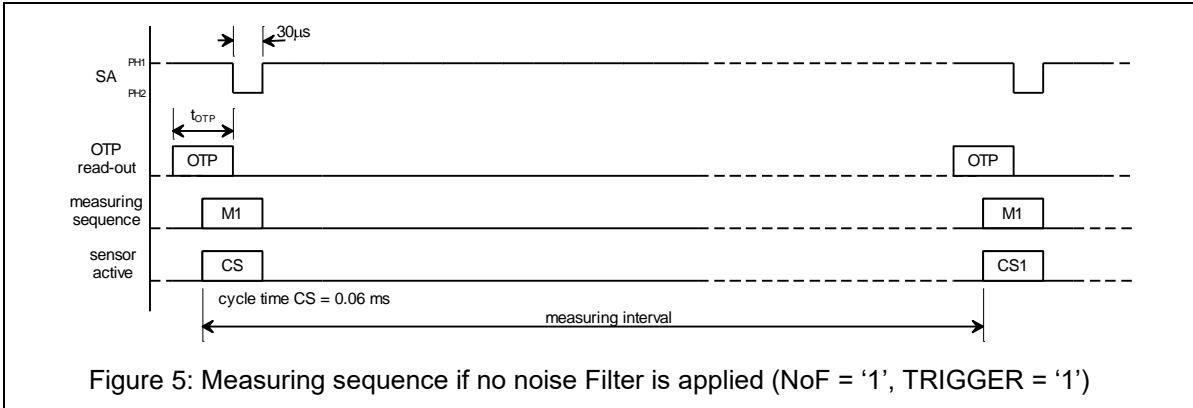
The state of the switch mode output signal CPF can be read via the I<sup>2</sup>C serial interface

The external reset pin RSTN allows a reset from an attached controller or a watchdog circuit. Additionally, the reset duration can be extended in applications where noise or instability of the rising power-supply require a longer reset. The RSTN pin is internally connected with a pull-up resistor to VDD and the delay time can be defined by choosing the value of an externally connected capacitor CR to VSS.

**8.1.1 Measuring sequence in switch mode**

In switch mode the capacitance of the sensor is compared with a capacitance threshold. This is done by comparing charges. The result of the comparison is available at the output OUT or over the I<sup>2</sup>C serial interface. A measurement in switch mode is either started with a single trigger (over input pin

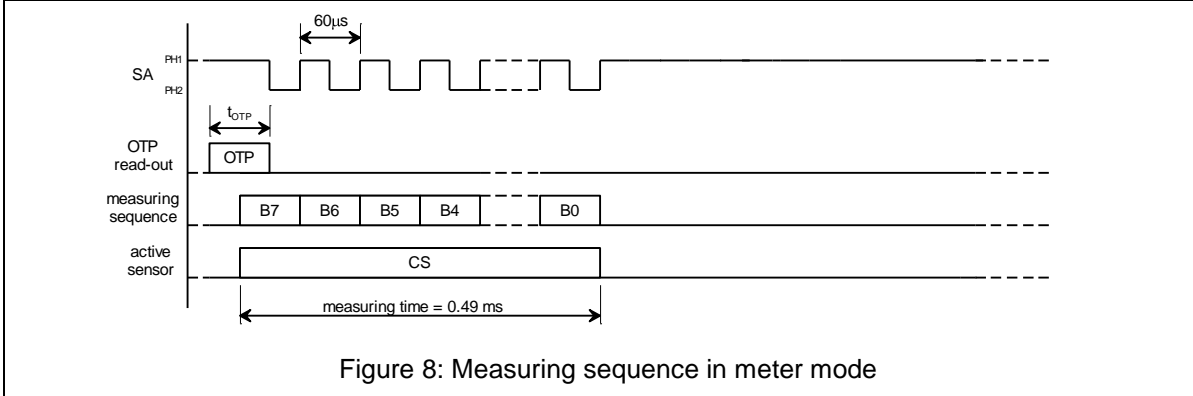
TRIGGER or by the I<sup>2</sup>C serial command COMP) or executed periodically. The measuring method and interval are defined by option MI in the options register OPT1 and by the logical value of pin TRIGGER. Each measuring phase has 1 (M1), 4 (M1 to M4) or 16 (M1 to M16) measuring cycles. The number of measuring cycles is defined by the level of the noise filter. The level of the noise filter is set according to option CF in the options register OPT1. The noise filter is switched off completely if option NoF (options register OPT2) is set to logical '1'. The evaluation result is available after the last measuring cycle. Figure 5, Figure 6 and Figure 7 show the measuring sequences for different filter levels.



The OTP memory read-out sequence is started ½ t<sub>OTP</sub> before the first measuring cycle M1 and stopped at the first falling edge of SA. The duration of t<sub>OTP</sub> is equal to one measuring cycle. The read-out of the OTP memory bits can be suppressed in RAM mode (register OPT2). This can be important for proper evaluation of the threshold capacitance. RAM mode is only possible if input TRIGGER is set to logical '1' (see 9.3.5 and 10.1).

**8.1.2 Measuring sequence in meter mode**

The meter mode is used to measure the absolute sensor capacitance of CS. The measured value of CS can be used to configure the fixed threshold of the switch mode or be used in a connected microcontroller for further evaluation. The meter mode is started by sending the command MCS to the MS8892A. Meter mode is only possible if input TRIGGER is set to logical '1' and the measuring interval MI in the options register OPT1 is set to single trigger or no trigger before applying the command MCS.



The command MCS runs through the measuring sequence as shown in Figure 8. The 8-bit digital capacitance value (B7 to B0) is evaluated with a successive approximation ADC via a binary search through all quantization levels. The measurement is finished after the measurement of the last bit (B0). The MS8892A enters the idle mode (oscillator disabled) after the end of the measurement.

**8.1.3 Threshold setting for switch mode measurement**

The MS8892A supports both, an absolute, fixed capacitance threshold and alternatively a relative threshold referencing to an automatically determined baseline capacitance, which takes manufacturing and material tolerances into account. The threshold mode is defined in the option THM in the register OPT2. The threshold value is defined in the register RTH, which has two different interpretations, depending on the threshold mode option THM:

- a) In the absolute threshold mode (option THM = '0'), RTH holds the 8-bit fixed threshold  $C_{TH}$  in the parameter  $FTH[7:0]$ .
- b) In the relative threshold mode (option THM = '1'), RTH holds the threshold polarity in bit STP and the threshold step size  $C_{STEP}$  in the parameter  $CSTEP[6:0]$  (the threshold step height).

The baseline capacitance value  $C_{BL}$  in the relative threshold mode corresponds to the capacitance value when the sensor is built into the target device and when it is not touched. Therefore, the baseline value  $C_{BL}$  takes into account variations of material properties (dielectric constant, thickness) and mechanical fabrication tolerances. The baseline is obtained by a regular capacitance measurement and is stored in the register CVAL.

THM	STP	Mode	Switching threshold
0	-	Absolute threshold	$C_{TH} = FTH[7:0]$
1	0	Relative threshold, negative step	$C_{TH} = CVAL[7:0] - CSTEP[6:0]$
1	1	Relative threshold, positive step	$C_{TH} = CVAL[7:0] + CSTEP[6:0]$

Table 3 Threshold capacitance in different modes

If an overflow or underflow occurs in the threshold calculation, the effective threshold is clamped to the respective maximum value (0xFF or 1000 fF) or minimum value (0x00 or 200 fF). An overflow or underflow error is visible in the result register RES, bit ERR (Section 0).

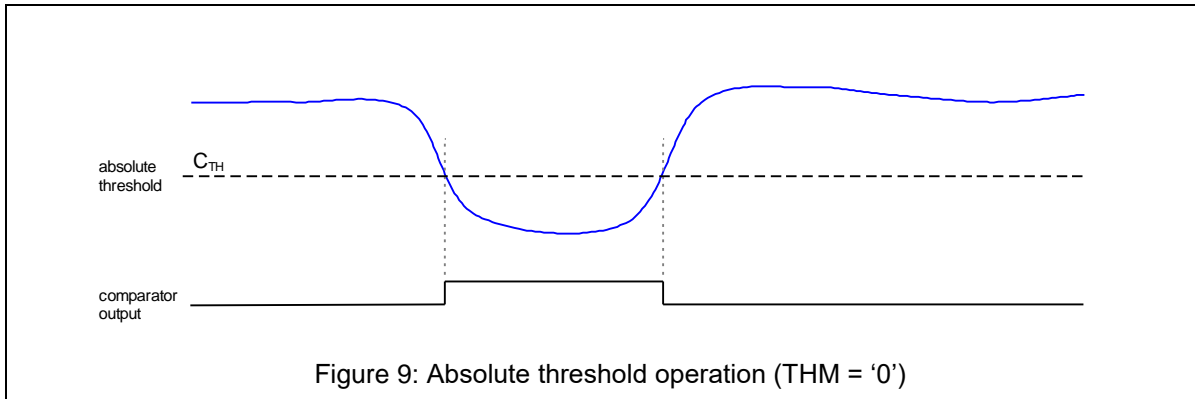


Figure 9: Absolute threshold operation (THM = '0')

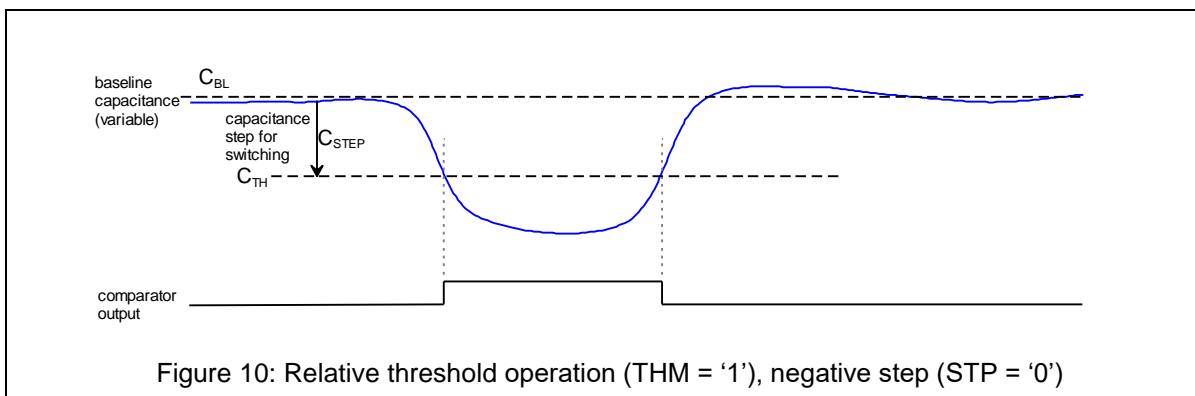


Figure 10: Relative threshold operation (THM = '1'), negative step (STP = '0')

The measurement of the baseline capacitance  $C_{BL}$  is executed in three situations: (1) immediately after power-up of the MS8892A in stand-alone operation, (2) by the I<sup>2</sup>C command MCS, and (3) by a positive pulse applied to the pin INIT. In periodic compare measurement mode (TRIGGER = 1 and MI ≠ '00' or TRIGGER = 0), the INIT pulse schedules the next measurement to be a baseline measurement, rather than a regular compare measurement. In single trigger mode (TRIGGER = 1 and MI = '00'), the INIT pulse immediately performs a baseline measurement.

Changing between absolute threshold mode and relative threshold mode is possible. The registers RTH and OPT1 must be programmed accordingly. To prevent false results due to periodic measurements during the mode change, it is suggested to put the device in single trigger mode before the threshold mode is reconfigured.

#### 8.1.4 Clock generation, external clock input and current consumption

The MS8892A supports two clock sources selectable by the option CLKS in register OPT1. The integrated oscillator is used as the main clock source, always controlling the measuring sequences. The oscillator runs nominally at  $f_{osc} = 32.8\text{kHz}$ .

If option CLKS = '0-' the internal oscillator runs continuously and controls the measuring interval when option MI is set to periodic measurements. The oscillator is not needed to control the measuring interval if the measuring interval MI is set to single trigger. In this case the oscillator is switched off at the end of the measuring sequence and the MS8892A enters the idle state.

If option CLKS = '1-' the external clock input on pin CLKIN is selected to control the measuring intervals defined in MI. In this case the internal oscillator is powered down even in the periodic measurement modes, and is only started to perform the actual measuring sequences. Two nominal frequencies are supported on CLKIN, 1024 Hz and 8192 Hz. If the CLKIN frequency differs from the selected nominal frequency, the measuring intervals change accordingly.

The current consumption is highest during the measurement sequence where measurement blocks are active. In periodic measurement modes, the power consumption is dominated by the oscillator power consumption. This consumption can be reduced using the external clock input if an external ultra-low power oscillator is available in the system, for example an RTC.

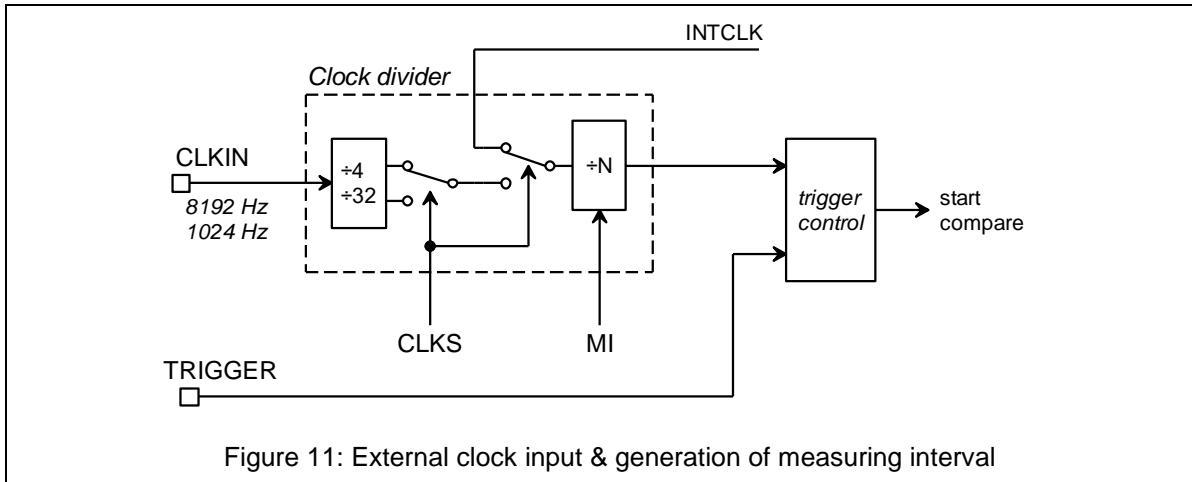


Figure 11: External clock input & generation of measuring interval

**8.1.5 Single hardware trigger in switch mode**

Pin TRIGGER can be used to trigger a single compare measurement. A negative pulse at pin TRIGGER of duration  $t_{TRG}$  activates a single trigger. A single measuring sequence is started after the time  $t_{TRG}$ . A trigger of a single measurement is only possible if the measuring interval MI is set to single trigger.

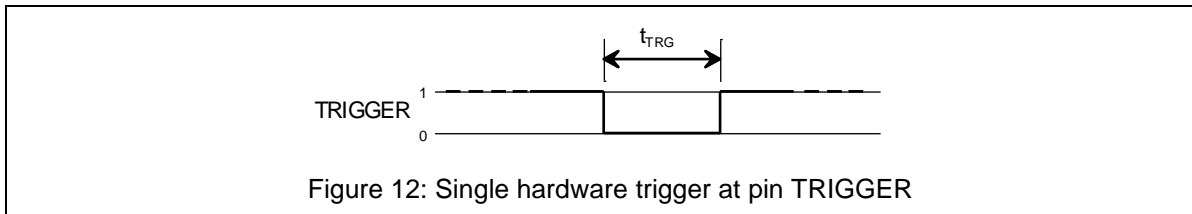


Figure 12: Single hardware trigger at pin TRIGGER

**8.1.6 Single software trigger in switch mode**

Command COMP executes a single compare measurement. A trigger of a single measurement is only possible if the measuring interval MI is set to single trigger and pin TRIGGER is set to logical '1'.

**8.1.7 Stand-alone operation in switch mode<sup>1</sup>**

After programming the non-volatile memory, the MS8892A can be used in switch mode without control of a microcontroller. Pin TRIGGER must be set to logical '0' for periodic measuring interval or to logical '1' for single trigger operation.

Pin TRIGGER set to logical '0' automatically starts a compare measurement about 30ms after power-up. This first measurement reads-out the non-volatile memory and sets the programmed options. The following measurements are executed according to the programmed interval. The measuring interval is 32 measurements per seconds if the measuring interval MI is not programmed (MI[1:0] = '00')

Registers RTH, OPT1 and OPT2 are always overwritten by the non-volatile memory contents prior to a measurement if pin TRIGGER is set to logical '0'.

**8.1.8 Measuring range**

The capacitance measuring range covers 0.2 pF to 1.0 pF with an ADC/DAC resolution of 3.1 fF (256 steps). The capacitance measurements in the meter mode have an 8-bit result, which is stored in the register CVAL.

**8.1.9 Noise filter and polarity selection**

The output CP of the comparator is input to the polarity selection and the digital noise filter. The polarity of the comparator output CP can be inverted by the bit POL in register OPT2.

<sup>1</sup> In stand-alone operation with TRIGGER set to logical '0', the OTP read-out is not functioning reliably in silicon version MS8892A. Therefore, the stand-alone mode is not correctly operating and should not be used. This problem will be corrected in the following version MS8892B.

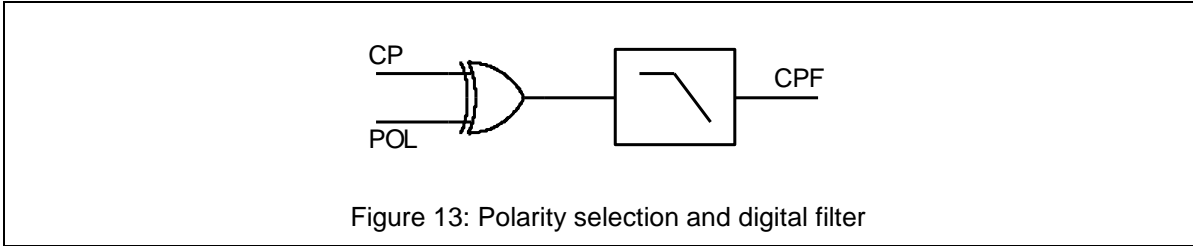


Figure 13: Polarity selection and digital filter

POL	CPF
0	CP
1	NOT CP

Table 4: Polarity selection

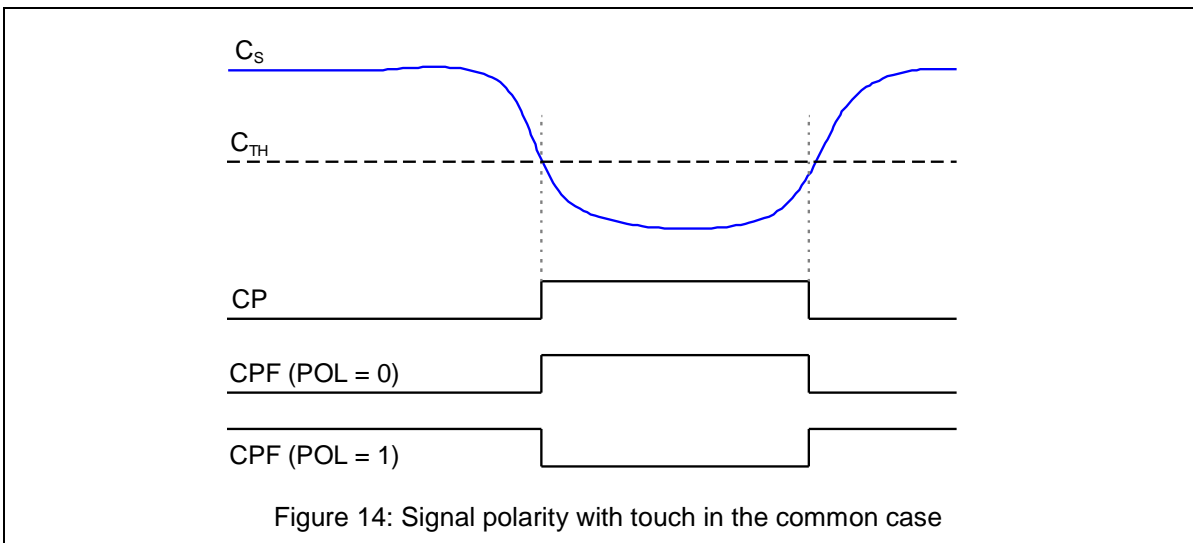


Figure 14: Signal polarity with touch in the common case

Figure 14 illustrates the polarity selection for the common case, where a touch event reduces the sensor capacitance value  $C_s$ . In this situation a touch causes a high-level at the comparator output CP. If there is no polarity inversion (POL = '0'), also the signal CPF after the filter is high-active, which results in a high active output OUT and high active bit CPF in the result register RES.

If a low-active output is required – in particular for the open-drain output mode (DRV = '1') – the polarity of CPF must be inverted by setting the option bit POL = '1'.

In the filter, three different levels of noise suppression can be selected:

- No noise filter  
The noise filter is switched-off if option NoF in the options register OPT2 is set. Option NoF overrules the settings made with option bit CF. The noise filter can only be disabled with option bit NoF if pin TRIGGER is set to logical '1'.
- Noise suppression CF = low  
4 measurements are performed per measurement phase. The signal at the output of the noise filter (CPF) changes the state if at least 3 measurements per measurement phase are equal (= 3 detections). The signal at the output of the noise filter remains at its previous state otherwise.
- Noise suppression CF = high  
16 measurements are performed per measurement phase. The signal at the output of the noise filter (CPF) changes the state if at least 12 measurements per measurement phase are equal (= 12 detections). The signal at the output of the noise filter remains at its previous state otherwise.



Noise suppression	NoF	CF	Measurements	Minimum number of detections	Measuring duration
No	1	-	1	1	0.06 ms
Low	0	0	4	3	0.24 ms
High	0	1	16	12	0.98 ms

Table 5: Noise suppression

Note: The measuring duration does not include the OTP read-out time (see section 8.1.1).

**8.1.10 Hysteresis**

The comparator has a built-in hysteresis as an additional noise filter. The amplitude of the hysteresis is equal to +/- CU. CU is the unit capacitance and typically 3.1 fF. The hysteresis is switched off in meter mode and is also switched off when the noise filter is switched off (input TRIGGER = '1' and option bit NoF = '1').

**8.1.11 Measuring interval**

In switch mode the measuring sequence can be executed on demand (single trigger) or periodically. The minimum measuring interval is given by the duration of the measurement sequence plus 1/2 t<sub>OTP</sub>, which must be obeyed in single trigger mode.

In periodic mode, three nominal measuring intervals of 32, 8 or 2 measurements per second are supported to allow a trade-off between reaction time and power consumption. The measuring intervals are directly influenced by the clock frequency of the internal oscillator respectively the external clock source.

If the clock frequency f<sub>CLKIN</sub> in external clocking mode differs from its nominal value of either 1024 Hz or 8192 Hz, the measuring intervals differ accordingly. This property of the MS8892A can be used to generate arbitrary measuring intervals by applying a custom f<sub>CLKIN</sub> frequency.

MI	Nominal measuring rate	Maximum reaction time
00	Single trigger	n/a
01	32 measurements / s	32 ms
10	8 measurements / s	125 ms
11	2 measurements / s	0.5 s

Table 6 Measuring intervals and reaction time

**8.1.12 Output logic, latching and driver**

Signal CPF is the output of the digital noise filter and input to the output logic with the adjacent output driver. Option bits OLM, DRV and PUE (register OPT2) control the behavior of the output stage.

Option DRV defines the driver mode of the output. The output driver mode can be CMOS (output is driven active low or active high) or open-drain (output is driven active low only; high level must be achieved by the internal or an additional external pull-up resistor).

DRV	Driver OUT
0	CMOS push-pull
1	Open-drain, low-active

Table 7: Output driver mode

In open-drain driver mode, option PUE enables or disables the internal pull-up resistor on pin OUT (R1 in Figure 15). If the internal pull-up resistor is enabled and OUT is driven to low level, the resistor gets disconnected from OUT with the switch P2 in order to avoid static power dissipation.

PUE	Internal pull-up
0	Internal pull-up disabled
1	Internal pull-up enabled in open-drain driver mode (DRV = '1')

Table 8 Internal pull-up resistor mode

Option OLM defines the latching mode of the output stage. If the latching mode is enabled, each activation of the sensor is stored in the latch and the output will keep its state even when the sensor is de-activated again. Only active-low signals are stored in the latch.

In the most common cases, a finger or object touching the sensor leads to a reduction of the sensor capacitance  $C_S$ . In this situation a touch is detected in switch mode when  $C_S < C_{TH}$ , which leads to a positive output CP of the comparator CP1 (Figure 4). In order to use the latching output mode, which is low active, it is required to inverse the signal polarity of CPF by setting option POL = '1'.

The latching state can be cleared by the I<sup>2</sup>C command LCLR or by pulling the input pin INIT to logical '1' for longer than  $t_{CLR}$ .

OLM	Driver OUT
0	Direct output mode, not latching
1	Latching output mode

Table 9: Output latching mode

In open-drain driver mode, also an external circuit can pull the signal OUT low. If this is the case, the low state will also be stored in the latch, and OUT will remain driven low until the latch is cleared again. The latching output mode is mainly used for the ultra-low power wake-up feature. For further information see section 11.2.

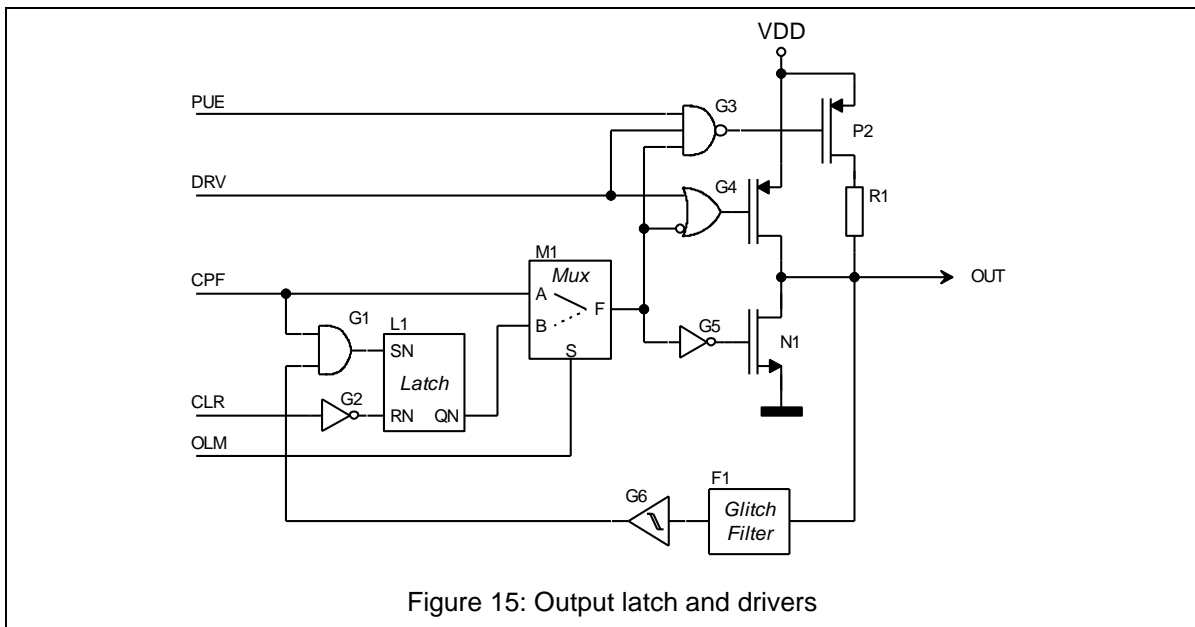


Figure 15: Output latch and drivers

Output driver mode and state	OLM	DRV	CPF	OUT
Direct output (not latching), CMOS push-pull driver	0	0	0	0
			1	1
Direct output (not latching), open-drain driver		1	0	0
			1	pulled-up
Latching enabled, CMOS push-pull driver	1	0	0	0
			1	0 (latch set) 1 (latch cleared)
Latching enabled, open-drain driver		1	0	0
			1	0 (latch set) pulled-up (latch cleared)



Table 10: Logic behaviour of the output stage  
(if PUE = '1' or an external pull-up resistor is attached to OUT)

## 9 I<sup>2</sup>C interface

The MS8892A has a slave receiver/transmitter I<sup>2</sup>C serial interface. SDA is data I/O and SCL is clock. SDA is used as an input or as an open-drain output. It is actively pulled low and must be passively held high by the external pull-up resistors on the I<sup>2</sup>C bus.

### 9.1 Supported I<sup>2</sup>C protocol

The following symbol set is used in the subsequent figures showing the I<sup>2</sup>C protocol.

- **S** = START symbol
- **Sr** = START repeated
- **P** = STOP symbol
- **A** = Acknowledge bit
  -  = sent from I<sup>2</sup>C slave
  -  = sent from I<sup>2</sup>C master

#### 9.1.1 Addressing

The I<sup>2</sup>C slave address has 7 bits. The slave address of the MS8892A is shown in the following table.

Bit	A6	A5	A4	A3	A2	A1	A0
Value	0	1	0	0	1	0	A0

Table 11: Selectable I<sup>2</sup>C slave address of MS8892A

The lowest address bit is defined by the logic level on the pin A0. In this way, two MS8892A instances can be addressed on a single I<sup>2</sup>C bus, at the 7-bit addresses 0x24 and 0x25.

#### 9.1.2 I<sup>2</sup>C master writes command

This protocol is used, if the I<sup>2</sup>C master only needs to send a single command to the MS8892A without additional data. The 8-bit command C7 to C0 is transmitted in the first data byte.

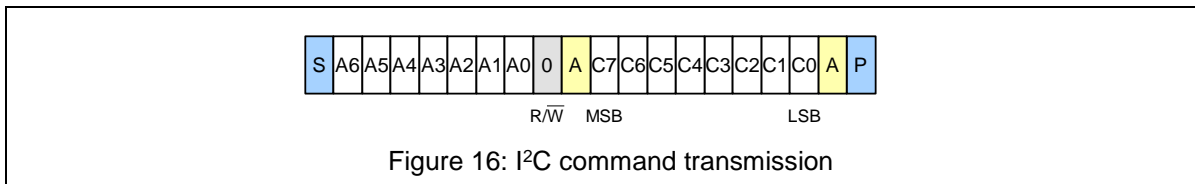


Figure 16: I<sup>2</sup>C command transmission

#### 9.1.3 I<sup>2</sup>C master writes one byte

This protocol is used, when the I<sup>2</sup>C master needs to program a register. The command part (C7 to C0) specifies the write register command including the selection of the register. The data byte (D7 to D0) contains the register content to be written.

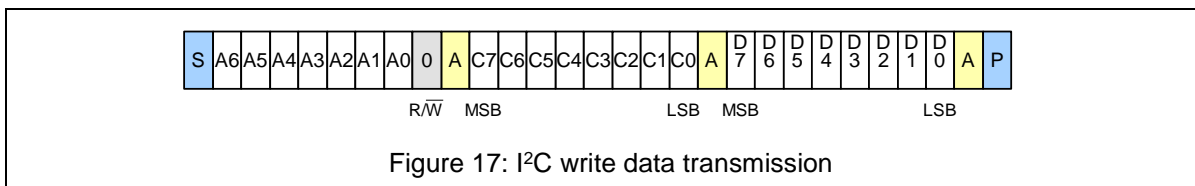


Figure 17: I<sup>2</sup>C write data transmission

#### 9.1.4 I<sup>2</sup>C master reads one byte

In order to read a register, the I<sup>2</sup>C master first has to send the corresponding read command. Therefore, the transmission starts with a command-write sequence. The transmission is not stopped after this. A repeated start is sent followed by a retransmission of the address. In this second part the R/W bit is set to logical high, indicating to the slave that it must transmit the data byte.

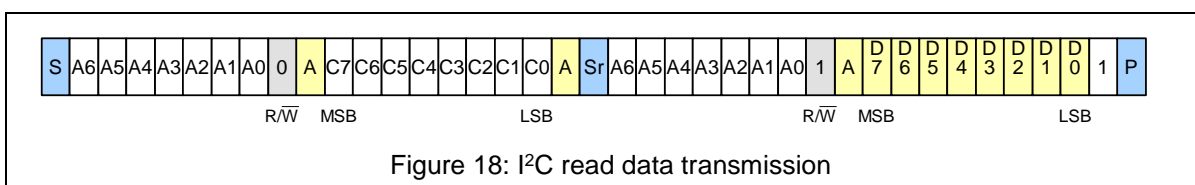


Figure 18: I<sup>2</sup>C read data transmission

## 9.2 I<sup>2</sup>C command table

Table 12 is a list of all allowed commands. Other commands are not allowed.

Command byte (C7 to C0)	Symbol	Function	Transfer type
00h	MCS <sup>2 3</sup>	Measure CS	Command
01h	RCS	Read CS (register CVAL)	Read 1 byte
02h	COMP <sup>2</sup>	Compare (switch mode)	Command
03h	RRES	Read comparison results (register RES)	Read 1 byte
04h	LCLR	Clear output latch	Command
05h	WTH	Write register RTH	Write 1 byte
06h	RTH	Read register RTH	Read 1 byte
07h	WOPT1	Write register OPT1	Write 1 byte
08h	ROPT1	Read register OPT1	Read 1 byte
09h	WOPT2	Write register OPT2	Write 1 byte
0Ah	ROPT2	Read register OPT2	Read 1 byte
0Bh	PTH	Program register RTH to OTP memory	Command
0Ch	POPT1	Program register OPT1 to OTP memory	Command
0Dh	POPT2	Program register OPT2 to OTP memory	Command

Table 12: I<sup>2</sup>C command table

## 9.3 Register description

### 9.3.1 Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset value
CVAL	CVAL[7:0]								'0000 0000'
RTH	FTH[7:0]								'0000 0000'
	STP	CSTEP[6:0]							
OPT1			CLKS[1:0]		MI[1:0]		NoF	CF	'0000 0000'
OPT2		THM	PUE	OLM	POL	DRV	INT	RAM	'0x00 0000'
RES					ERR	LATS	LAS	CPF	'xxxx x000'

Table 13: Register overview

### 9.3.2 CVAL: Capacitance value of sensor CS, lower 8 bits

Bit(s)	Symbol	Function	Reset value
7:0	CVAL[7:0]	Capacitance value of sensor CS (lower 8 bits B7..B0). The value is binary coded. The LSB value is defined by the unit capacitance CU (Section 8.1.8) This value serves also as the baseline value for the threshold in the automatic threshold setting mode.	'0000 0000'

Table 14: Description of CVAL – capacitance value of sensor CS

<sup>2</sup> Before sending the next command after an MCS or COMP command, a waiting time of  $\geq 2$  ms is required for the completion of the measurement.

<sup>3</sup> A measurement in meter mode is only executed if the measuring interval MI is set to single trigger. The CVAL register will not change its content if an MCS command is issued during periodic compare measurements.

### 9.3.3 RTH: Fixed threshold capacitance or relative threshold step size for sensor CS

The RTH register has two interpretations. If the MS8892A is configured for a fixed absolute threshold (THM = '0' in register OPT2), then RTH contains the 8 bits FTH[7:0] of the fixed threshold capacitance. When the relative threshold mode is enabled (THM = '1' in register OPT2), then RTH contains the threshold step polarity bit (STP) and the 7-bit relative threshold step height (CSTEP).

Bit(s)	Symbol	Function	Reset value
7:0	FTH[7:0]	Absolute threshold capacitance value for sensor CS in switch mode (lower 8 bits). The value is binary coded. The LSB value is defined by the unit capacitor CU (Section 8.1.8)	'0000 0000'

Table 15: Description of RTH (THM = '0') – threshold capacitance for sensor CS

Bit(s)	Symbol	Value	Function	Reset value
7	STP	'0' '1'	Relative threshold step polarity negative threshold step positive threshold step	'0'
6:0	CSTEP[6:0]		Relative threshold step height. The value is binary coded. The LSB value is defined by the unit capacitor CU (Section 8.1.8) This value is added/subtracted to/from the threshold baseline value in CVAL to determine the switching threshold in relative threshold mode.	'000 0000'

Table 16: Description of RTH (THM = '1') – threshold step height

### 9.3.4 OPT1: Options register 1

Bit(s)	Symbol	Value	Function	Reset value
7:6	n/a	n/a	n/a	n/a
5:4	CLKS[1:0]	'0-' '10' '11'	Clock source selection - internal oscillator (32 kHz) - external clock input, 1024 Hz - external clock input, 8192 Hz	'00'
3:2	MI[1:0]	'00' '01' '10' '11'	Measuring interval - single trigger - periodic, 32 measurements per second - periodic, 8 measurements per second - periodic, 2 measurements per second	'00'
1	NoF	'0' '1'	Noise filter switched on Noise filter switched off	'0'
0	CF	'0' '1'	Noise suppression low (3/4 detections) high (12/16 detections) Note: Bit NoF overrules this setting	'0'

Table 17: Description of OPT1 – options register 1

### 9.3.5 OPT2: Options register 2

Bit(s)	Symbol	Value	Function	Reset value
7	n/a	n/a	n/a	n/a
6	THM	'0' '1'	Absolute / relative threshold mode absolute threshold mode relative threshold mode	'0'
5	PUE	'0' '1'	Enable for internal pull-up resistor on OUT pin Internal pull-up disabled Internal pull-up enabled if in open-drain configuration (DRV = '1')	'0'
4	OLM	'0' '1'	Output latching mode Direct output mode, not latching Latching output mode	'0'
3	POL	'0' '1'	Output polarity selection not inverted, OUT is high if $C_S < C_{TH}$ inverted, OUT is high if $C_S > C_{TH}$	'0'

2	DRV	'0' '1'	CMOS output driver (OUT) Open-drain output driver (OUT)	'0'
1	INT	'0' '1'	Interrupt over I <sup>2</sup> C bus Interrupt mode disabled Interrupt if CPF state changes	'0'
0	RAM	'0' '1'	Source of configuration ROM mode: RTH, OPT1, OPT2 are overwritten by corresponding OTP memory registers prior to measurement RAM mode: RTH, OPT1, OPT2 are never overwritten prior to measurement Note: The RAM bit is not written to or read from OTP	'0'

Table 18: Description of OPT2 – options register 2

### 9.3.6 RES: Comparison result & latching state register

Bit(s)	Symbol	Value	Function	Reset value
7:4	n/a		n/a	n/a
3	ERR	'0' '1'	Relative threshold calculation error state Valid threshold calculation result Overflow (positive threshold step) or underflow (negative threshold step) has occurred in threshold calculation <sup>4</sup>	'0'
2	LATS	'0' '1'	Latching trigger source (when LAS = '1') Output latching triggered internally by touch event Output latching triggered externally by pulling OUT low	'0'
1	LAS	'0' '1'	Output latching state Output latch clear Output latch activated, OUT pulled active low Note: Output latching mode is only enabled when DRV = '1' and OLM = '1'. Otherwise LAS = '0'	'0'
0	CPF	'0' '1'	Comparison result sensor CS C <sub>S</sub> > C <sub>TH</sub> (POL = '0') C <sub>S</sub> < C <sub>TH</sub> (POL = '0') Note: The output value is inverted with POL = '1'	'0'

Table 19: Description of RES – comparison result &amp; latching state

<sup>4</sup> Section 8.1.3 describes the threshold setting for switch mode measurements. If an overflow occurs in the relative threshold calculation, the resulting threshold value is clamped to the value of 0xFF corresponding to 1000 fF. If an underflow occurs, the resulting threshold value is clamped to the value of 0x00 corresponding to 200 fF

**9.4 Interface timing**

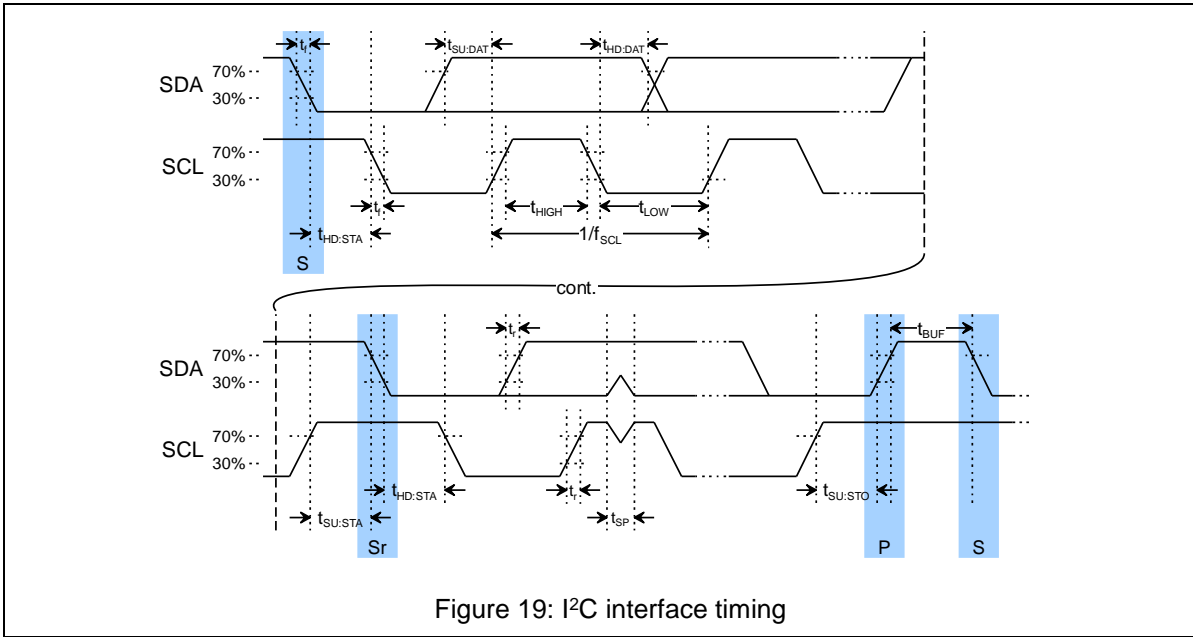


Figure 19: I<sup>2</sup>C interface timing

Note: The timing figures are specified in section 12.

**9.5 Interrupt over I<sup>2</sup>C bus<sup>5</sup>**

In order to flag a switching event – corresponding to a level change of the internal signal CPF – over the I<sup>2</sup>C bus, the MS8892A can behave like an I<sup>2</sup>C master with restricted functionality. A CPF level change is signaled by sending a START condition, immediately followed by a STOP condition. This is illustrated in Figure 20. No further I<sup>2</sup>C master capabilities are supported.

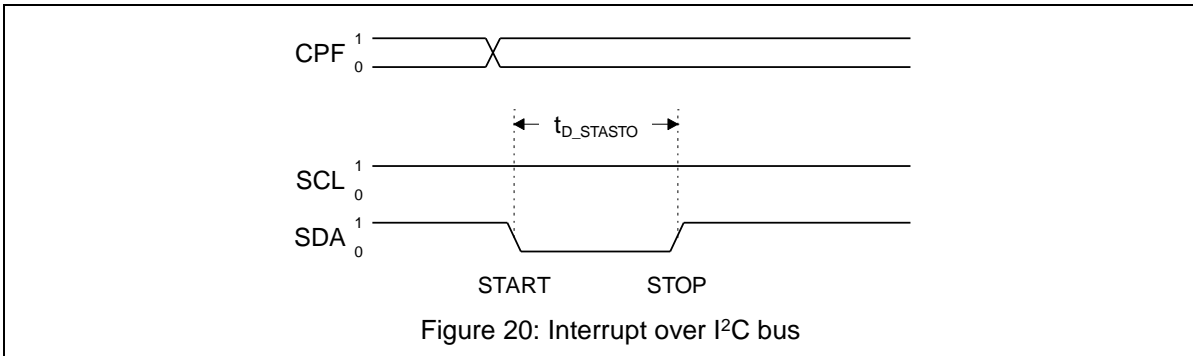


Figure 20: Interrupt over I<sup>2</sup>C bus

The I<sup>2</sup>C master has to detect the START-STOP condition and react accordingly. In order to enable this mode, the MS8892A has to be set into interrupt mode in register OPT2.

<sup>5</sup> Instead of signalling each level change of the CPF signal, the interrupt-over-I2C pulse is only generated when output OUT changes. This problem will be corrected in the following version MS8892B

**10 OTP memory**

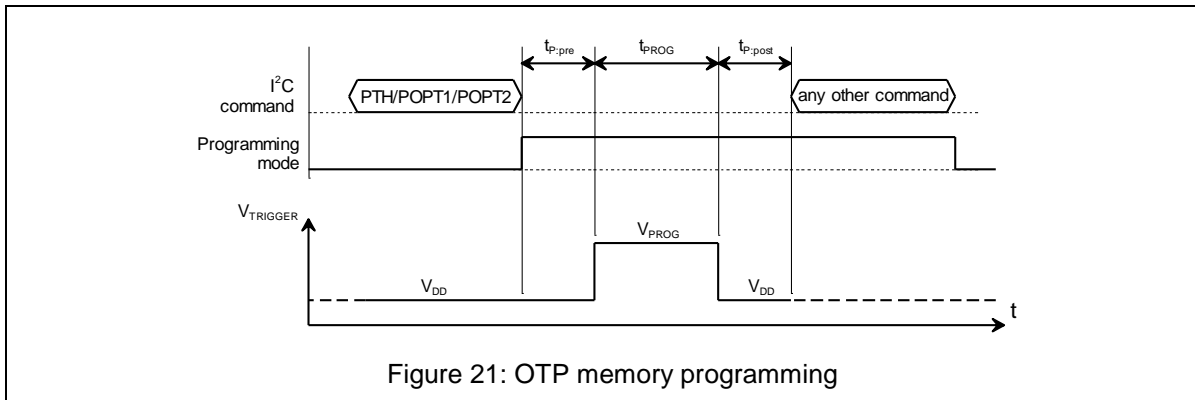
**10.1 RAM or ROM operation**

Option RAM in the register OPT2 defines if the configuration registers RTH, OPT1 and OPT2 are overwritten by the corresponding OTP memory registers prior to each measurement. The default logical state of option RAM is '0' after power-up. This means that the registers are overwritten from the OTP memory prior to measurement. Before changing any of the registers RTH, OPT1 or OPT2 option RAM must be set to logical '1'. This guarantees that the volatile registers RTH, OPT1 and OPT2 are not overwritten again by the OTP memory contents prior to any measurement. Option RAM can only be set if pin TRIGGER is set to logical '1'.

**10.2 OTP programming**

After setting the registers RTH, OPT1 and OPT2 the register contents can be programmed to the OTP memory. These registers must be programmed to the OTP memory if the MS8892A needs to function stand-alone. The OTP memory bits can be programmed once from logical '0' to logical '1'. Once programmed, they cannot be reset to logical '0' anymore.

The OTP programming sequence is started with one of the commands PTH (OTP programming of register RTH), POPT1 (OTP programming of register OPT1) or POPT2 (OTP programming of register OPT2). These commands enable the programming mode. The non-volatile programming of the OTP memory bits is then done by applying a programming pulse at pin TRIGGER with voltage  $V_{PROG}$  and duration  $t_{PROG}$ . The programming mode must be left latest after the OTP programming of the last register. This is done by sending any I<sup>2</sup>C command except PTH, POPT1, POPT2 to the MS8892A.





11 Application information

11.1 Basic sensor design

Many parameters define the sensor’s capacitance value and its sensitivity. It is therefore not possible to give exhaustive design guidelines. The following design guidelines are meant as a starting point for the application specific sensor design. More details are given in the MS8892A application note (separate document).

Figure 22 shows a basic sensor layout. The sensor capacitor has two electrical conductors SA and SB. SA is the transmitter and SB is the receiver. The transmitter SA surrounds the receiver as much as possible. This gives the highest capacitance and also the highest immunity to noise. The sensor’s capacitance is increased by increasing the sensor’s antenna length  $l_b$ . The sensor’s capacitance is also increased by lowering the distance  $d$  between the transmitter and the receiver and by increasing the SA and SB conductor widths  $w_a$  and  $w_b$ .

It is important to shield (e.g. with VSS lines and/or a VSS grid) the receiver antenna between the MS8892A package pins and the sensor area. The shielding capacity must not exceed 5pF. If properly shielded, the sensor is only sensitive at the sensor area and also the capacitance is only defined by the sensor area.

Figure 23 shows the typical sensor’s relative capacitance value as a function of the distance to an object. The sensor capacitance is changed if an object (e.g. finger) is approaching the sensor area. The dependence between sensor capacitance and distance to the object depends on many parameters and must be evaluated in the application. A small distance  $d$  between SA and SB reduces the relative sensitivity for objects at large distances (curve A is almost flat for large distances). And a large distance  $d$  between SA and SB increases the relative sensitivity for objects at large distances (curve B is steeper than curve A for larger distances).

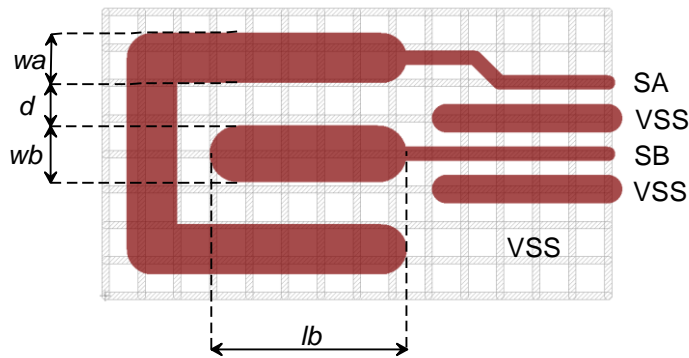


Figure 22: Basic sensor layout

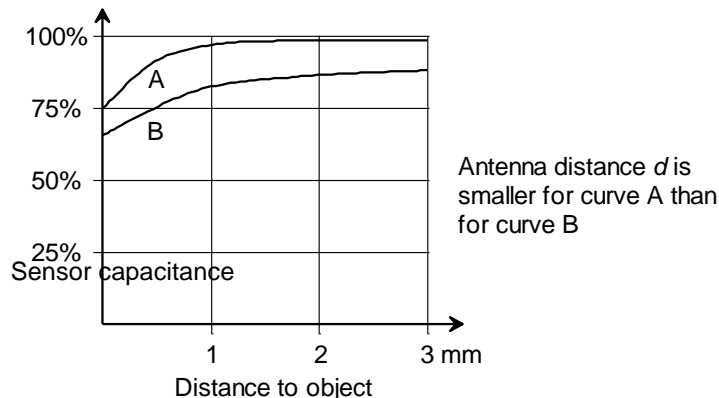
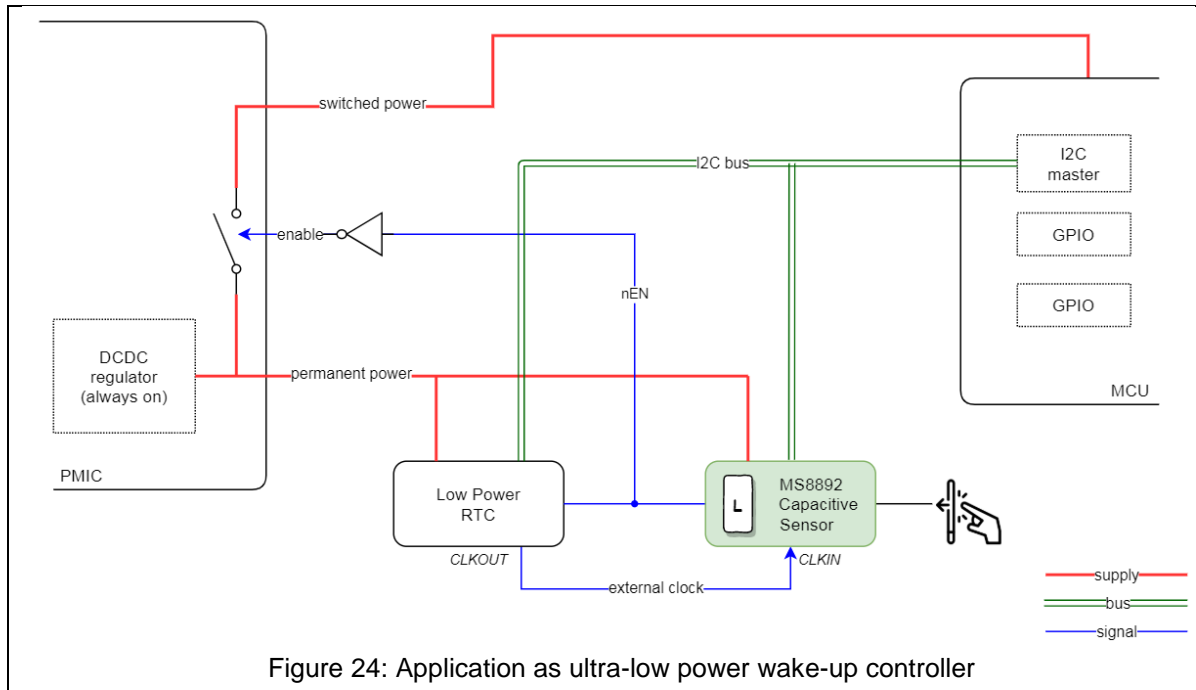


Figure 23: Sensor capacitance as a function of the distance to the object

The sensor capacitance and the relative capacitance change can be optimized with capacitance simulations of different sensor layouts.

## 11.2 Application as ultra-low power wake-up controller

Figure 24 illustrates the application of the MS8892A as an ultra-low power wake-up controller.



The system consists of a power management IC (PMIC), a system controller (MCU), and the two wake-up sources capacitive touch sensor MS8892A (green) and the real-time clock (RTC). For simplicity, other system elements like sensors, memories, RF modules etc., which are connected to the MCU, are not explicitly shown in the diagram.

The MCU and the rest of the system are supplied by a switched power supply. Disabling the system power enables the lowest possible power consumption in power off mode, in which even the leakage current of the system is avoided.

Wake up sources from this power off mode are the capacitive touch sensor MS8892A and the RTC. A touch event or an RTC alarm enable the system power by controlling a switch in the PMIC. The outputs of the MS8892A and the RTC are both low-active open-drain types and are connected together (signal nEN).

A high level on signal nEN is achieved by a pull-up resistor. To reduce external components, the MS8892A contains an internal pull-up resistor, which can be optionally enabled. If the signal nEN is driven to logic low level by the MS8892A, the internal pull-up resistor is disconnected to avoid the static current flow. This is a further method to reduce power consumption in ultra-low power systems.

The system power state is kept in the internal latch 'L' in the MS8892A. The latch 'L' will be set (thus switching on the switched power via enable) by a touch event or when the RTC pulls the signal nEN low due to an alarm.

After power-up the MCU is in control and can read out the wake-up source from the MS8892A. It can re-configure the parameters of the MS8892A and the alarm settings of the RTC.

The system will return to the power off mode by clearing the latch in the MS8892A, which in turn disables the switched power supply. The latch can be cleared by an I<sup>2</sup>C command or an optional hardware signal from a GPIO of the MCU to the INIT pin of the MS8892A (not shown in the diagram).

In this application example, further power is saved by clocking the MS8892A from a permanent clock signal from the RTC (external clock). This allows the internal oscillator of the MS8892A to be disabled.

## 12 Electrical Characteristics

### 12.1 Limiting values and ESD protection

Name	Parameter	Min	Max	Unit
V <sub>DD</sub>	Positive supply voltage wrt to V <sub>SS</sub>	-0.5	9.0	V
V <sub>I</sub>	Input voltages wrt to V <sub>SS</sub>	-0.5	V <sub>DD</sub> +0.5	V
I <sub>I</sub> , I <sub>O</sub>	Input and output currents	-10	10	mA
I <sub>VSS</sub>	Total current to V <sub>SS</sub>	-25	25	mA
P <sub>TOT</sub>	Power dissipation		100	mW
T <sub>stg</sub>	Storage temperature	-60	+125	°C
T <sub>J</sub>	Junction temperature		+125	°C
V <sub>ESD</sub>	Electrostatic discharge voltage (HBM JS-001-2017)		+/- 2000	V

Table 20: Limiting values<sup>6</sup> and ESD protection<sup>7</sup>

### 12.2 DC characteristics

Conditions: V<sub>DD</sub> = 3V, T<sub>amb</sub> = 25°C, if not stated otherwise

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>DD</sub>	Positive supply voltage		1.8		4.5	V
I <sub>DD,INT</sub>	Operating current, internal oscillator	Idle state, oscillator disabled		50		nA
		Idle state, oscillator enabled, MI = periodic		720		nA
		Active current during measurement		11		µA
		Average current (switch mode), 2 measurements/s, CF = low		735		nA
		Average current (switch mode), 32 measurements/s, NoF = '1'		800		nA
		Average current (switch mode), 32 measurements/s, CF = low		860		nA
		Average current (switch mode), 32 measurements/s, CF = high		1.1		µA
I <sub>DD,INT</sub>	Operating current, external clock source	Idle state, oscillator disabled, f <sub>CLKIN</sub> = 8.192 kHz		tbd		nA
		Idle state, oscillator disabled, f <sub>CLKIN</sub> = 1.024 kHz		tbd		nA
		Average current (switch mode), 2 measurements/s, CF = low, f <sub>CLKIN</sub> = 8.192 kHz		tbd		nA
		Average current (switch mode), 2 measurements/s, CF = low, f <sub>CLKIN</sub> = 8.192 kHz		tbd		nA
		Average current (switch mode), 32 measurements/s, CF = low, f <sub>CLKIN</sub> = 1.024 kHz		tbd		nA
		Average current (switch mode), 32 measurements/s, CF = low, f <sub>CLKIN</sub> = 1.024 kHz		tbd		nA
		Average current (switch mode), 32 measurements/s, CF = low, f <sub>CLKIN</sub> = 1.024 kHz		tbd		nA

<sup>6</sup> These are stress ratings only. Stress above one or more of the limiting values may cause permanent damage to the device. Operation of the device at these or at any other conditions above those given in the characteristics section of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

<sup>7</sup> Inputs and outputs are protected against electrostatic discharge during normal handling. However to be totally safe, it is advisable to undertake precautions appropriate to handling MOS devices.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<i>Sensor capacitance</i>						
CS <sub>typ</sub>	Typical range of sensor capacitance		200		1000	fF
CU	ADC resolution		2.95	3.1	3.25	fF
<i>OTP memory programming characteristics</i>						
V <sub>PROG</sub>	OTP programing voltage	Device in OTP programming mode	9.9	10.0	10.1	V
<i>Digital inputs (A0, CLKIN, INIT, SCL, SDA, RSTN)</i>						
V <sub>IL</sub>	Input low level for digital inputs		V <sub>SS</sub>		0.3V <sub>DD</sub>	V
V <sub>IH</sub>	Input high level for digital inputs		0.7V <sub>DD</sub>		V <sub>DD</sub>	V
R <sub>RSTN</sub>	Pull-up resistor on RSTN			153		kΩ
<i>Digital input / output (OUT)</i>						
V <sub>OL</sub>	Output low level for digital outputs	I <sub>OUT</sub> = 2mA	V <sub>SS</sub>		0.2V <sub>DD</sub>	V
V <sub>OH</sub>	Output high level for digital outputs	I <sub>OUT</sub> = -2mA, DRV = '0'	0.8V <sub>DD</sub>		V <sub>DD</sub>	V
I <sub>OUT</sub>	Output current	DRV = '0'	-5		5	mA
R <sub>OUT</sub>	Switchable pull-up resistor on OUT	DRV = '1' and PUE = '1'		175		kΩ
<i>Analog input (SB)</i>						
V <sub>AI</sub>			V <sub>SS</sub>		V <sub>DD</sub>	V
<i>I<sup>2</sup>C interface pins</i>						
V <sub>O:SDA</sub>	Output low level on SDA	I <sub>SDA</sub> = 2mA	V <sub>SS</sub>		0.2V <sub>DD</sub>	V
<i>Temperature range</i>						
T <sub>amb</sub>	Operating temperature range		-40	25	85	°C

Table 21: DC characteristics

## 12.3 AC characteristics

 Conditions:  $V_{DD} = 3V$ ,  $T_{amb} = 25^{\circ}C$ , if not stated otherwise

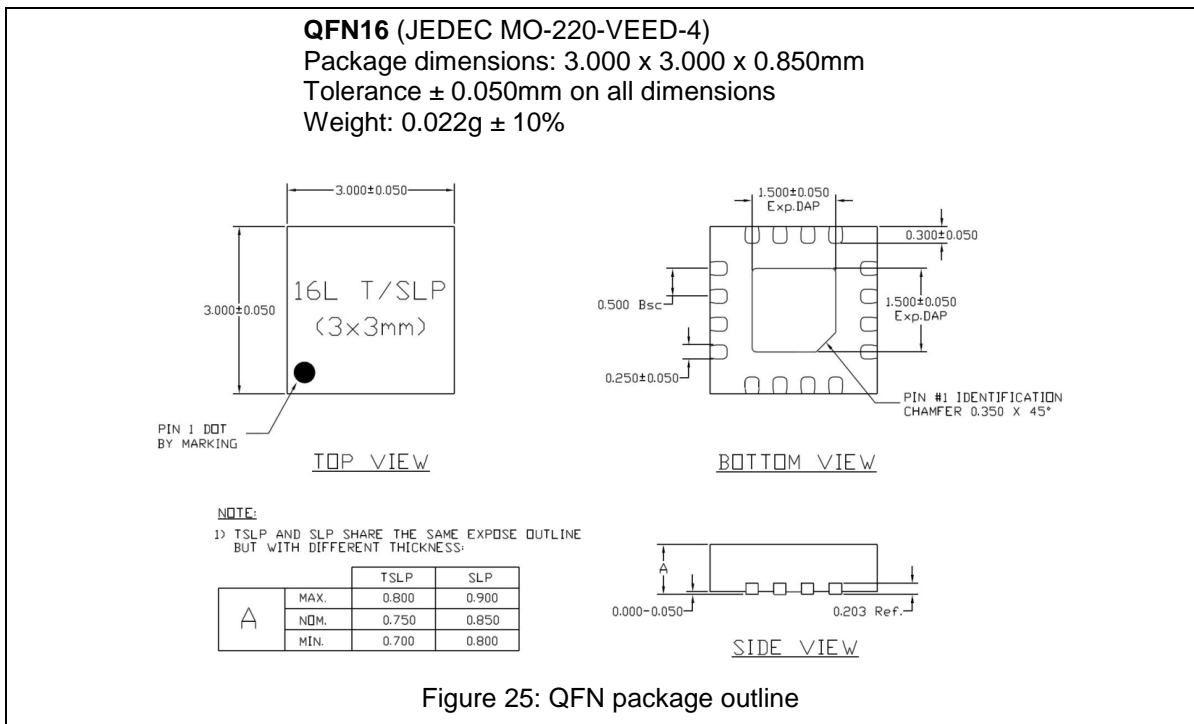
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f <sub>OSC</sub>	Oscillator frequency		30	32.8	35.6	kHz
t <sub>meas:sw</sub>	Measuring time for single measurement cycle in switch mode	NoF = '1'		0.06		ms
		NoF = '0', CF = '0'		0.24		ms
		NoF = '0', CF = '1'		0.98		ms
t <sub>meas:meter</sub>	Measuring time for single measurement sequence in meter mode			0.49		ms
f <sub>MI</sub>	Measuring rate in switch mode	MI[2:0] = '01'		32		Hz
		MI[2:0] = '10'		8		Hz
		MI[2:0] = '11'		2		Hz
f <sub>CLKIN</sub>	External clock frequency	CLKS[1:0] = '10'		1024		Hz
		CLKS[1:0] = '11'		8192		Hz
t <sub>OTP</sub>	OTP read-out time			0.06		ms
t <sub>TRG</sub>	External single trigger		1	50	100	μs
t <sub>NOF</sub>	Delay of polarity change	Polarity change of pin TRIGGER '0' to '1' or '1' to '0'			2	ms
t <sub>BLM</sub>	External baseline measurement trigger pulse	Positive pulse on pin INIT	1	50	100	μs
t <sub>LCLR</sub>	Delay of latch clearing	Polarity change of pin INIT '0' to '1'			2	ms
t <sub>RSTN</sub>	Power-on reset duration	C <sub>RSTN</sub> = 1 nF		175		μs
		C <sub>RSTN</sub> = 100 nF		17.5		ms
<i>OTP programming characteristics</i>						
t <sub>PROG</sub>	OTP programming pulse		95	100	105	ms
t <sub>p:pre</sub>	Time between end of OTP programming command and start of OTP programming pulse		0.1			ms
t <sub>p:post</sub>	Time between end of OTP programming pulse and start of next I <sup>2</sup> C command		0.1			ms
<i>I<sup>2</sup>C interface characteristics (SDA, SCL)</i>						
t <sub>SP</sub>	Pulse width of spikes that must be suppressed		0		100	ns
f <sub>SCL</sub>	SCL clock frequency		0		100	kHz
t <sub>HD:STA</sub>	Hold time (repeated) START condition		4.0			μs
t <sub>SU:STA</sub>	Setup time (repeated) START condition		4.7			μs
t <sub>LOW</sub>	LOW period of the SCL clock		4.7			μs
t <sub>HIGH</sub>	HIGH period of the SCL clock		4.0			μs
t <sub>HD:DAT</sub>	Data hold time		50			ns
t <sub>SU:DAT</sub>	Data setup time		250			ns
t <sub>r</sub>	Rise time SDA, SCL				1	μs
t <sub>f</sub>	Fall time SDA, SCL				0.3	μs
t <sub>SU:STO</sub>	Setup time for STOP condition		4.0			μs
t <sub>BUF</sub>	Bus free time between START and STOP		4.7			μs
t <sub>D:STASTO</sub>	Duration of interrupt over I <sup>2</sup> C bus pulse on SDA line	Interrupt mode enabled		3		μs

Table 22: AC characteristics

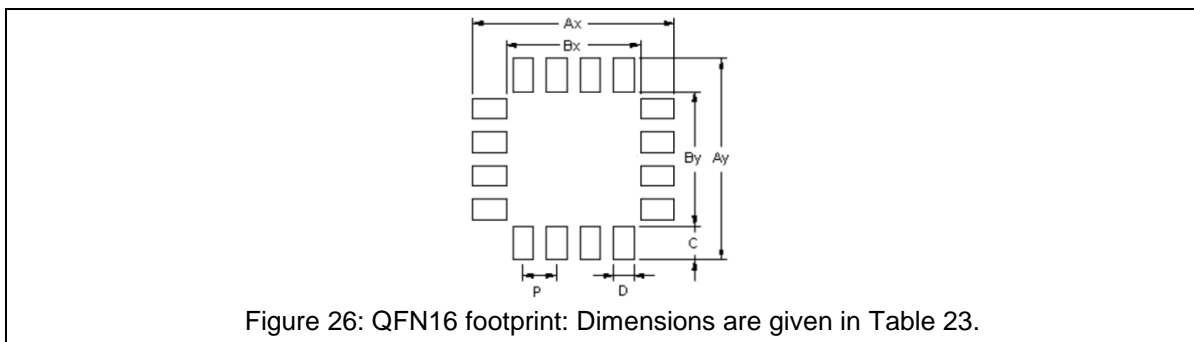
## 13 Production note

### 13.1 QFN16

#### 13.1.1 QFN16 package outline



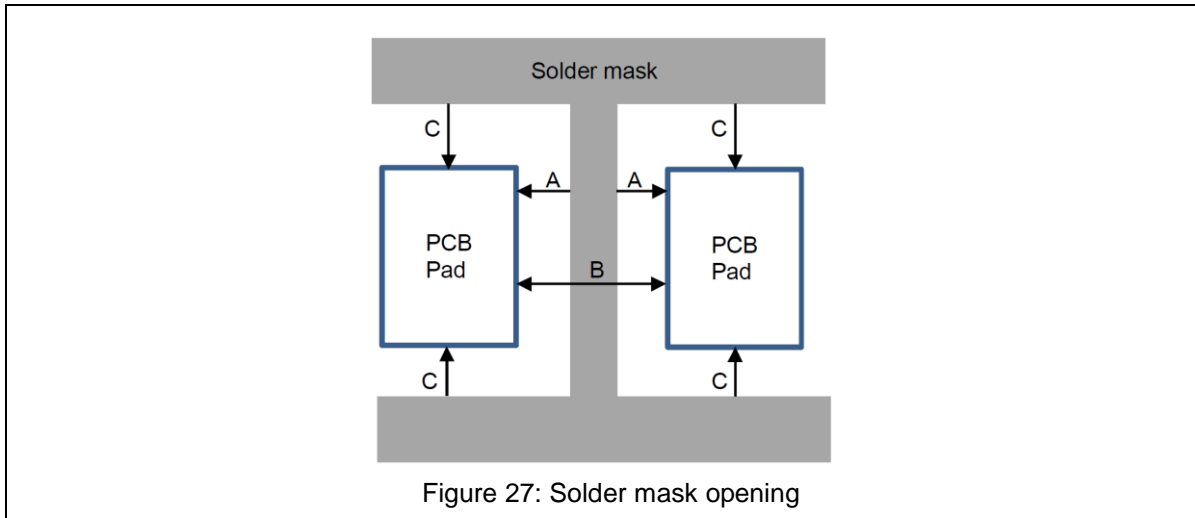
#### 13.1.2 PCB design



Symbol	Value	Tolerance	Unit
P	0.5	$\pm 0.03$	mm
Ax	3.8	$\pm 0.03$	mm
Ay	3.8	$\pm 0.03$	mm
Bx	2.1	$\pm 0.03$	mm
By	2.1	$\pm 0.03$	mm
C	0.85	$\pm 0.03$	mm
D	0.3	$\pm 0.03$	mm

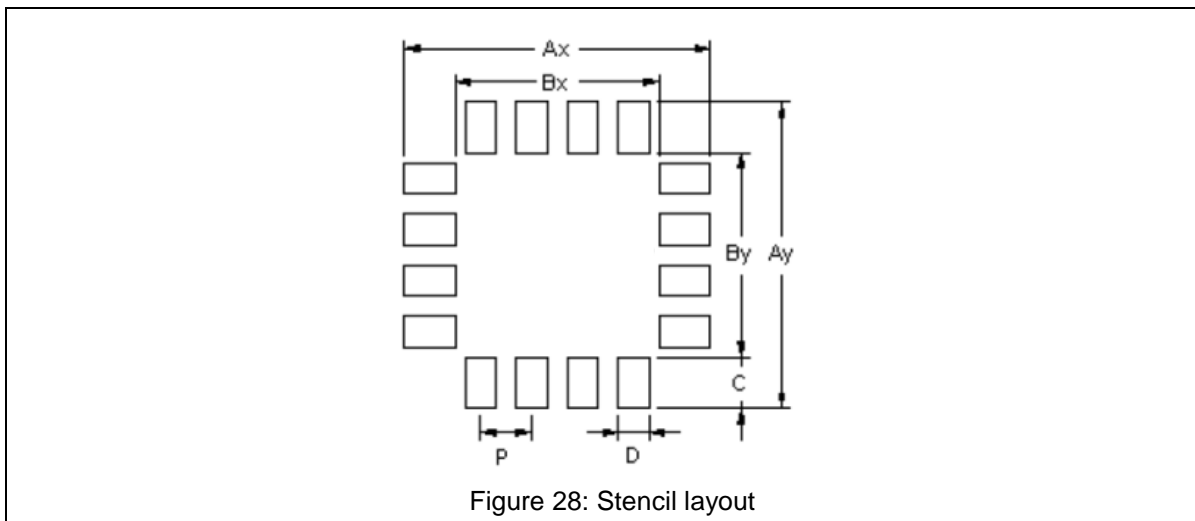
Table 23: QFN16 footprint dimensions

Solder mask opening for PCB area: If necessary, the edge of the solder mask opening around the PCB pads can be set up to the edge of the pad (A). If the distance between the pads is insufficient for the solder mask (B) then the mask can be set to the bottom and the top edges of the pads (C).



### 13.1.3 Assembly instructions

The recommended stencil thickness is 0.10 to 0.13mm. Refer to Figure 28 and Table 24 for layout and dimensions.



Symbol	Value	Tolerance	Unit
P	0.5	±0.03	mm
Ax	3.64	±0.03	mm
Ay	3.64	±0.03	mm
Bx	2.28	±0.03	mm
By	2.28	±0.03	mm
C	0.68	±0.03	mm
D	0.24	±0.03	mm

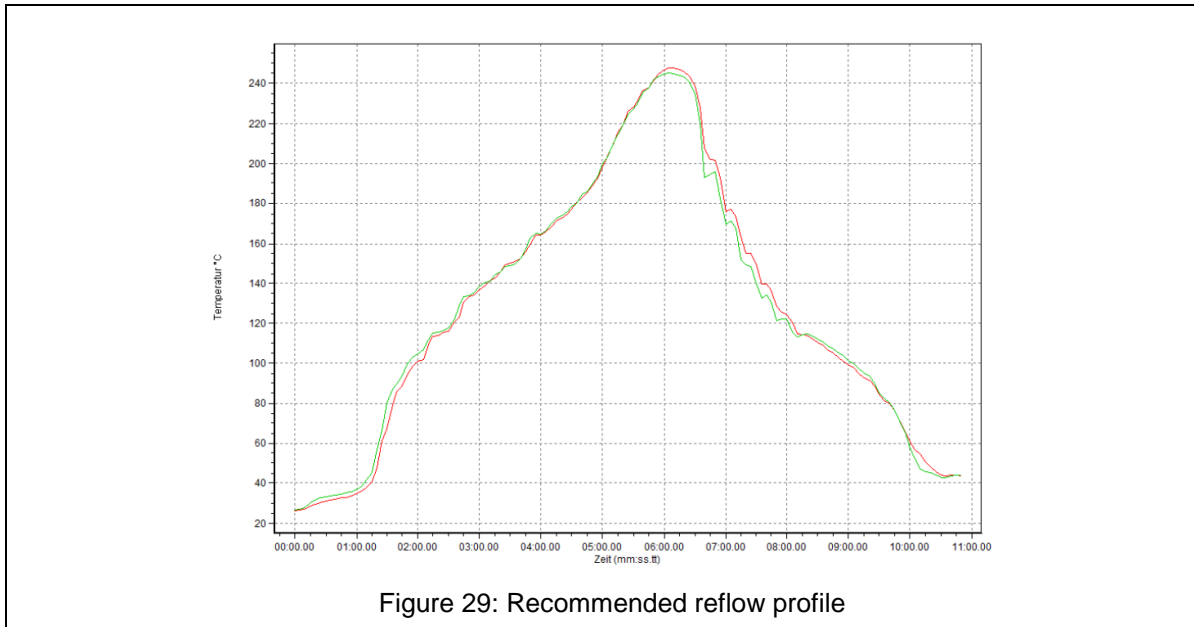
Table 24: Stencil dimensions

The recommendations in the table above are based on a stencil thickness of 0.10 to 0.13mm and the PCB footprint size given in section 13.1.2. The stencil dimensions are 80% of the footprint size. Both the stencil thickness and dimensions are recommendations. The stencil thickness and dimensions may have to be adjusted to take into account other components on the board. For example, components with leads may typically require a little more solder to compensate for co-planarity problems. Generally speaking increasing the stencil thickness and/or dimensions result in more solder being deposited and

increases the risk of bridging. Decreasing the stencil thickness and/or dimensions results in less solder being deposited and increases the risk of insufficient solder for a good solder joint.

### 13.1.4 Recommended reflow parameters

The reflow profile is dependent on many different parameters. The profile here is given as a guide. It may be necessary to adjust the profile slightly depending on the solder flux and equipment used. The key temperature/times associated with the different reflow oven zones are defined in J-STD-020.

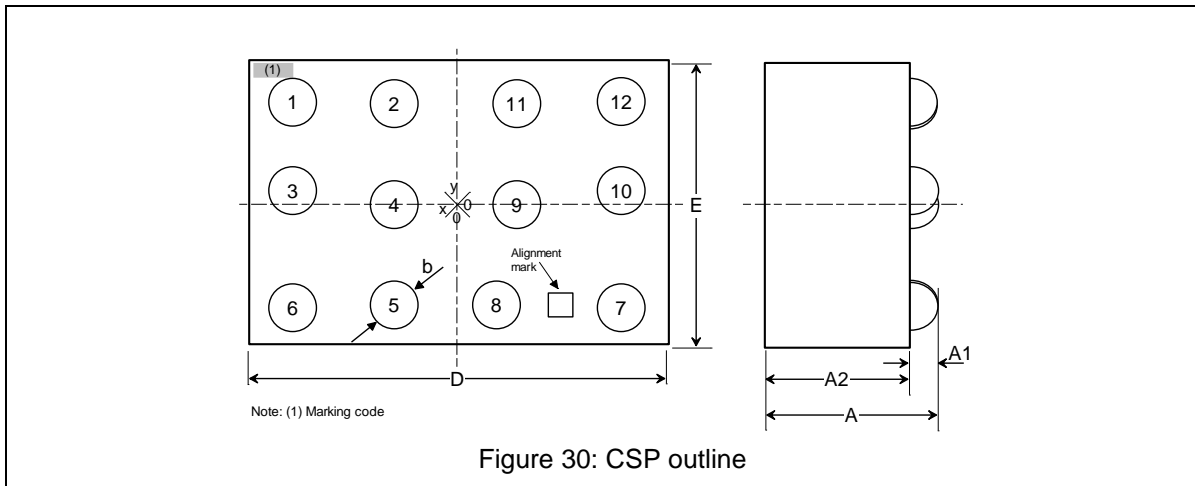


The maximum reflow temperature is 260°C. The moisture sensitivity level is 1 (MSL1).



## 13.2 CSP

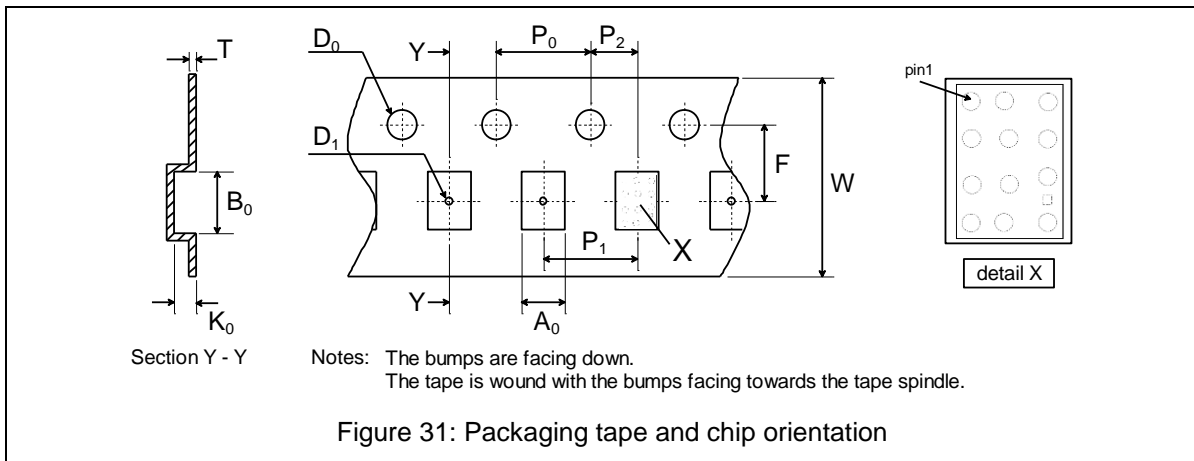
### 13.2.1 Bump coordinates and dimensions



Bump No.	X (μm)	Y (μm)	Item	Value	Tolerance
1 (SB2)	-595	360	Chip size (D)	1.52mm	±30μm
2 (VDD)	-225	355	Chip size (E)	1.03mm	±30μm
3 (POL)	-595	53	Chip thickness (A2)	525μm	±20μm
4 (TRIGGER)	-225	0	Bump height	100μm	±15μm
5 (VSS)	-225	-355	Bump height inclusive redistribution (A1)	112μm	±19μm
6 (SB1)	-595	-362	Chip thickness including bumps (A)	637μm	±39μm
7 (OUT1)	595	-362	Bump diameter (b)	172μm	±17μm
8 (OUT2)	150	-355	Bump placement	±3μm	
9 (SA1)	225	0	Bump material	Sn (97.5%) Ag (2.5%)	
10 (SA2)	595	53	Alignment mark	100μm x 100μm	
11 (SDA)	225	355			
12 (SCL)	595	360			
Alignment mark	375	-355			

Table 25: Solder bump coordinates and dimensions

## 13.2.2 Packaging tape

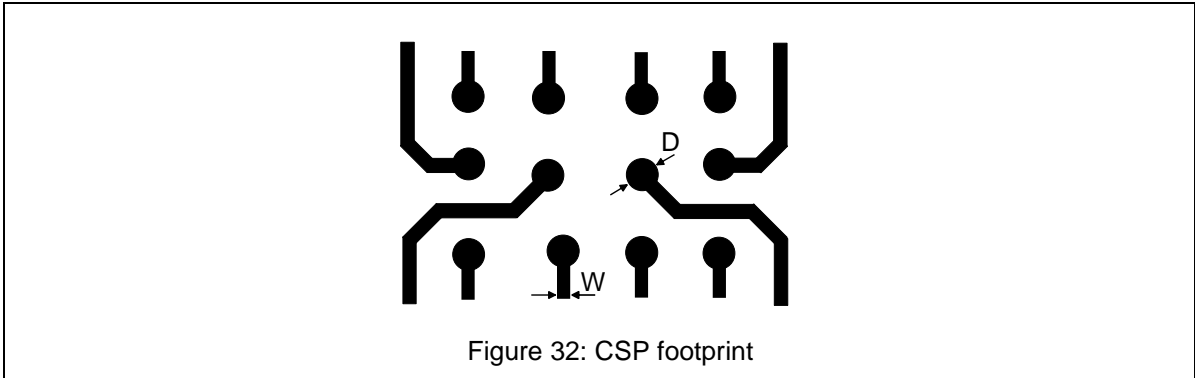


Symbol	Description	Value	Tol.	Unit
A <sub>0</sub>	Pocket x	1.20	±0.10	mm
B <sub>0</sub>	Pocket y	1.65	±0.10	mm
D <sub>0</sub>	Diameter sprocket hole	1.55	±0.05	mm
D <sub>1</sub>	Diameter pocket hole	0.55	±0.05	mm
F	Center of sprocket hole to center of pocket	3.5	±0.05	mm
K <sub>0</sub>	Pocket z	0.7	±0.05	mm
P <sub>0</sub>	Hole pitch	4.0	±0.10	mm
P <sub>1</sub>	Pocket pitch	4.0	±0.10	mm
P <sub>2</sub>	Pocket to sprocket hole pitch	2.0	±0.05	mm
T	Tape thickness	0.30	±0.05	mm
W	Tape width	8.0	±0.30	mm

Table 26: Tape dimensions for CSP package

**13.2.3 PCB design**

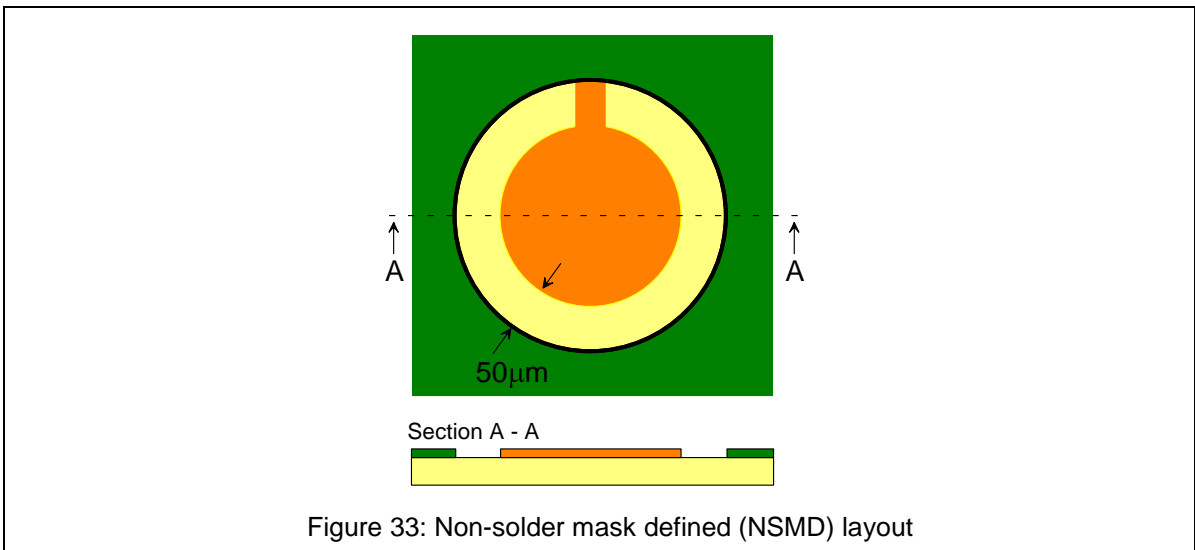
The values given in this section are recommendations for PCB designs with Ni/Au pad surface finish.



Symbol	Description	Value	Tol.	Unit
D	Pad diameter	220	±20	µm
W	Width of pad connection	100... 200		µm

Table 27: CSP footprint dimensions

It is recommended to use a non-solder mask defined (NSMD) layout for the PCB pads with a distance of 50µm between the PCB pad and the edge of the solder mask opening.



**13.2.4 Assembly instructions**

For solder paste deposition it is recommended to use an electropolished laser-cut stencil with a thickness of 80µm and a circular aperture with a diameter of 200µm.

It is recommended to use a type IV solder paste, preferably mildly activated (RMA), with a solder particle diameter of 20 to 38µm.

The assembly procedure for the CSP package is compatible with surface mount procedures.

The CSP package must be placed on the PCB using a pick and place machine with optical alignment. The alignment can be verified using the package outline. The misalignment must not exceed ±50µm in both directions.

The CSP package does not require underfill.

## 13.2.5 Recommended reflow parameters

The reflow profile is dependent on many different parameters. The profile here is given as a guide. It may be necessary to adjust the profile slightly depending on the solder flux and equipment used. The key temperature/times associated with the different reflow oven zones are defined in J-STD-020.

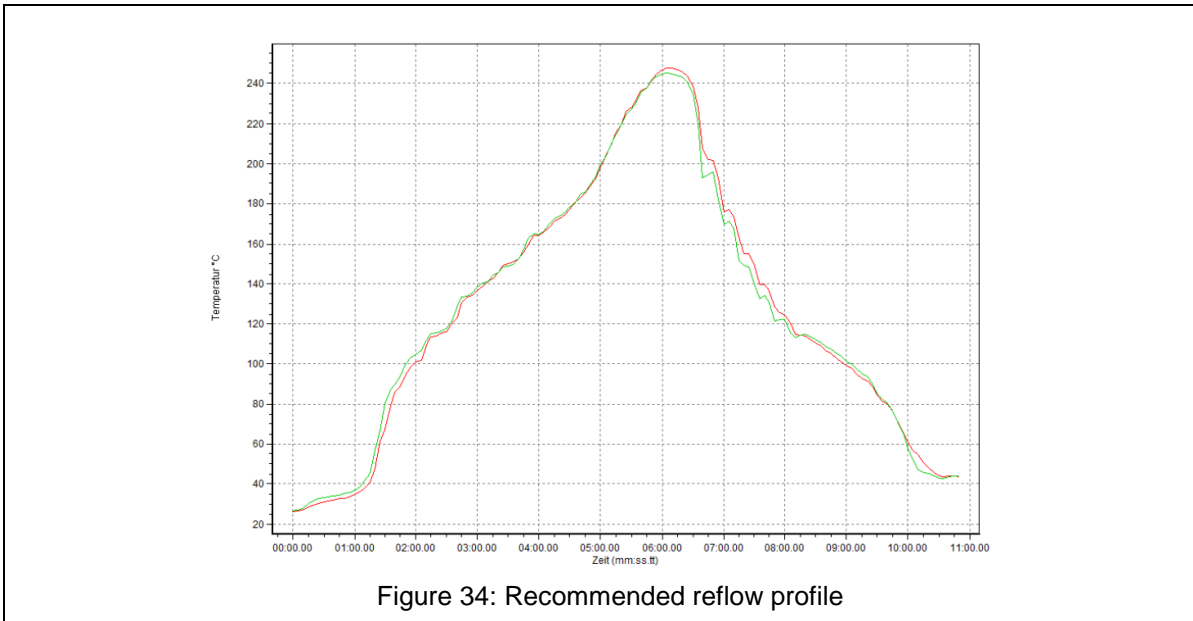


Figure 34: Recommended reflow profile

The maximum allowed reflow temperature is 260°C. The moisture sensitivity level is 1 (MSL1).

## 14 Legal disclaimer

This product is not designed for use in life support appliances or systems where malfunction of these parts can reasonably be expected to result in personal injury. Customers using or selling this product for use in such appliances do so at their own risk and agrees to defend, indemnify and hold harmless Microdul AG from all claims, expenses, liabilities, and/or damages resulting from such use of the product.

## 15 Contents

1	General Description .....	1
2	Typical application .....	1
3	Applications .....	1
4	Features .....	1
5	Ordering Information .....	2
6	Pinout .....	2
7	Pin description .....	2
8	Description .....	3
8.1	Basic functionality .....	3
9	I <sup>2</sup> C interface .....	11
9.1	Supported I <sup>2</sup> C protocol .....	11
9.2	I <sup>2</sup> C command table .....	12
9.3	Register description .....	12
9.4	Interface timing .....	15
9.5	Interrupt over I <sup>2</sup> C bus .....	15
10	OTP memory .....	16
10.1	RAM or ROM operation .....	16
10.2	OTP programming .....	16
11	Application information .....	17
11.1	Basic sensor design .....	17
11.2	Application as ultra-low power wake-up controller .....	18
12	Electrical Characteristics .....	19
12.1	Limiting values and ESD protection .....	19
12.2	DC characteristics .....	19
12.3	AC characteristics .....	21
13	Production note .....	22
13.1	QFN16 .....	22
13.2	CSP .....	25
14	Legal disclaimer .....	29
15	Contents .....	29