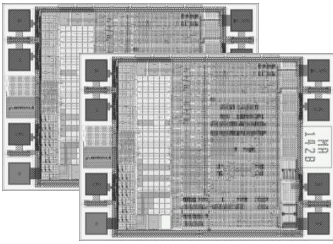


## Dual channel capacitive switch with auto-calibration, large voltage operating range and very low power



### 1 General Description

The integrated circuit MS8886C is a dual channel capacitive switch that uses a patented (EDISEN) digital method to detect a change in capacitance on a remote sensing plate.

Changes in the static capacitance (as opposed to dynamic capacitance changes) are automatically compensated using continuous auto-calibration. Remote sensing plates (e.g. conductive foil) can be connected to the IC using coaxial cable.

### 2 Applications

- Hermetically sealed keys on a keyboard
- Switch for medical applications
- Switch for use in explosive environments
- Vandal proof switches
- Automotive: Switches in or under upholstery, leather, handles, mats and glass
- Portable entertainment units
- Buildings: Switch in or under carpets, glass or tiles
- Sanitary applications: Use of standard metal sanitary parts (e.g. tap) as switch

### 3 Typical application

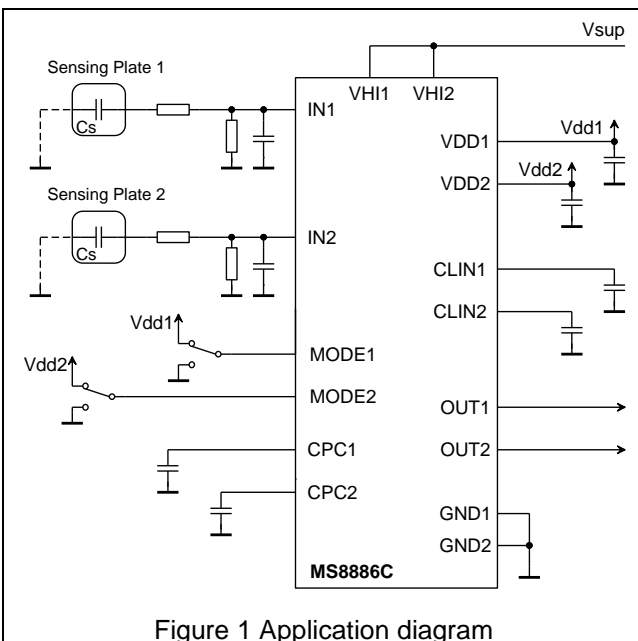


Figure 1 Application diagram

### 4 Features

- Dynamic proximity switch
- Digital processing method
- Automatic calibration
- Sensing plates can be connected remotely
- Open-drain output (P-type MOSFET, external load between pin and ground)
- Designed for battery powered applications ( $I_{HI}$  typ.  $6\mu A$ )
- Adjustable response time
- Adjustable sensitivity
- Independently configurable switching dynamics per channel
- Large voltage operating range ( $V_{HI} = 2.7$  to  $9V$ )
- Large temperature operating range ( $T_{amb} = -40$  to  $85^{\circ}C$ )
- Internal voltage regulator
- Available in 3x3mm QFN16 (other packages available for larger quantities)

### 5 Pinout

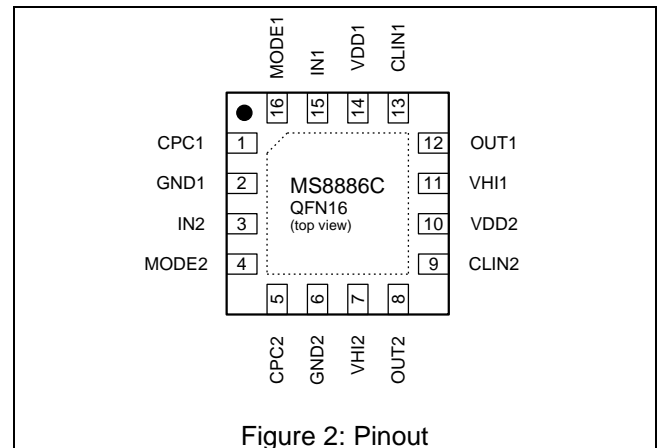


Figure 2: Pinout

### 6 Ordering Information

Table 1: Ordering information

Typ	Package	Shipping	Article No.
MS8886C	QFN16 3x3mm	Tape&Reel	9160179

## 7 Block diagram

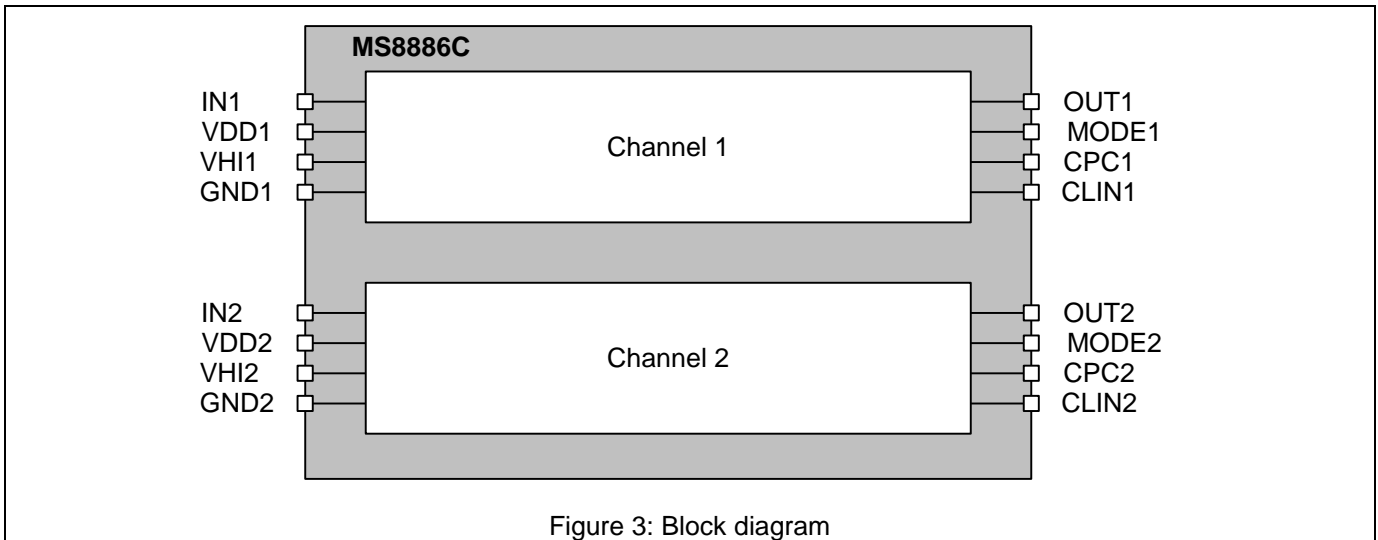


Figure 3: Block diagram

## 8 Pin description

Table 2: Pin description

Pin CSP	Pin QFN16	Symbol	I/O <sup>1</sup>	Description
1	15	IN1	I	Sensor-Input
2	16	MODE1	I	Switching behaviour definition
3	1	CPC1	A	Reservoir capacitor
4	2	GND1	S	Negative supply, should be connected to GND2
5	3	IN2	I	Sensor-Input
6	4	MODE2	I	Switching behaviour definition
7	5	CPC2	A	Reservoir capacitor
8	6	GND2	S	Negative supply, should be connected to GND1
9	7	VHI2	S	Positive supply
10	8	OUT2	O	Switch output
11	9	CLIN2	A	Oscillator capacitor
12	10	VDD2	S	Internal supply, must not be connected to VDD1
13	11	VHI1	S	Positive supply
14	12	OUT1	O	Switch output
15	13	CLIN1	A	Oscillator capacitor
16	14	VDD1	S	Internal supply, must not be connected to VDD2

<sup>1</sup> I: Input, O: Output, S: Supply, A: Analogue

## 9 Description

### 9.1 Basic functionality

The MS8886C consists of two identical, fully independent sensor channels. Each channel can be configured and operated separately. Each channel can be powered down by removing its VHI supply voltage independently.

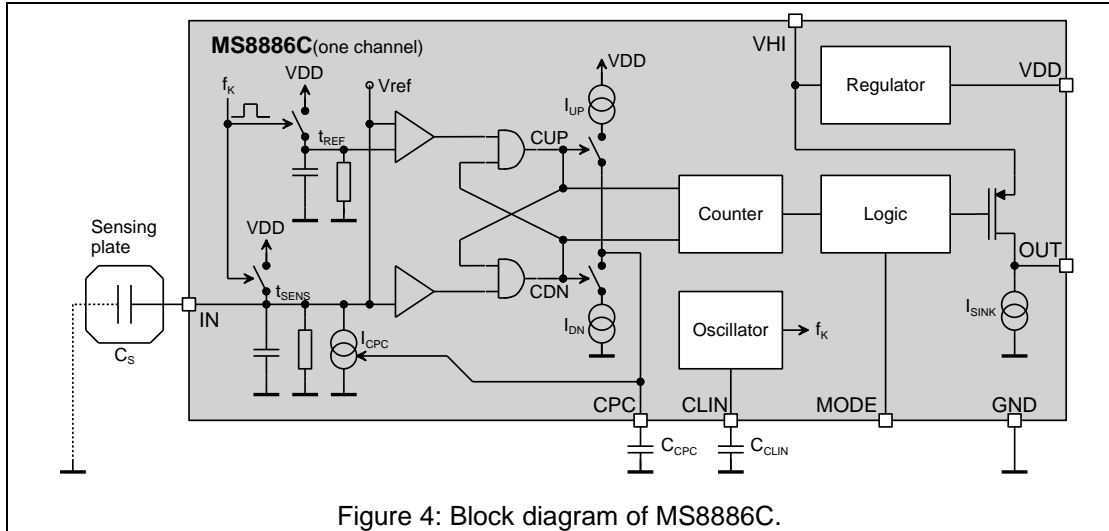


Figure 4: Block diagram of MS8886C.

Figure 4 illustrates the functional principle of one channel of the MS8886C.

The discharge time  $t_{SENS}$  on input pins IN[1:2] attached to the sensing plate capacitance is compared to the discharge time  $t_{REF}$  of an internal RC timing element. Both RC timing circuits are periodically charged to  $V_{DD}$ [1:2] level via MOS switches and then discharged via a resistor to ground (GND).

The charge discharge cycle is governed by the sampling rate ( $f_K$ ). When the voltage of an RC combination falls below the  $V_{REF}$  level, the appropriate comparator output will change. The logic following the comparators determines which comparator switched first. If the upper (reference) comparator switches, then a pulse is given on CUP. If the lower (input) comparator switches first then a pulse is given on CDN (see Figure 2).

The pulses control the charge on the external capacitors  $C_{CPC}$ [1:2] on pins CPC[1:2]. Every time a pulse is given on CUP, capacitor  $C_{CPC}$  is charged through a current source  $I_{UP}$  from  $V_{DD}$  for a fixed time causing the voltage on  $C_{CPC}$  to rise by a small increment. Likewise when a pulse occurs on CDN, capacitor  $C_{CPC}$  is discharged through a current sink  $I_{DN}$  towards ground for a fixed time, causing the voltage on  $C_{CPC}$  to fall by a small decrement.

The voltage on  $C_{CPC}$  controls an additional current sink  $I_{CPC}$  that causes the capacitance attached to the input pins IN[1:2] to be discharged more quickly. This arrangement constitutes a closed-loop control system, that constantly tries to equalise the discharge time  $t_{SENS}$  with  $t_{REF}$ . In the equilibrium state, the discharge times are equal and the pulses alternate between CUP and CDN.

The counter following this logic counts the pulses CUP or CDN respectively. The counter is reset every time the pulse sequence changes from CUP to CDN or vice versa. The output pins OUT[1:2] will only be activated when a sufficient number of consecutive CUP or CDN pulses occur. Low level interference or slow changes in the input capacitance do not cause the output to switch.

Various measures, such as asymmetrical charge and discharge steps, are taken to ensure that the output switches off correctly. Two different switching dynamics can be chosen by connecting the MODE[1:2] pins to either GND or  $V_{DD}$ [1:2].

A special start-up circuit ensures that the device reaches equilibrium quickly when the supply is attached.

Pins OUT[1:2] are open drain outputs capable of pulling an external load  $R_{OUT}$  (up to 20mA) up to  $V_{HI}$ . The load resistor must be dimensioned appropriately, taking the maximum expected  $V_{HI}$  voltage into account.

A small internal 150nA current sink  $I_{SINK}$  enables a full voltage swing to take place on pins OUT[1:2], even if no load resistor is connected. This is useful for driving purely capacitive CMOS inputs. The falling slope can be fairly slow in this mode, depending on load capacitance.

The sampling rate ( $f_k$ ) corresponds to half of the frequency generated in the internal sawtooth oscillator. The sampling rate can be adjusted within a specified range by selecting the value of the  $C_{CLIN}$  capacitor.

**9.2 Application notes**

Figure 3 shows the typical connections for a general application of one channel of the MS8886C. The positive supply (3.0V to 9.0V) is connected to pin  $V_{HI}$ . It is recommended to connect decoupling capacitors to ground for both  $V_{HI}$  and  $V_{DD}$ .

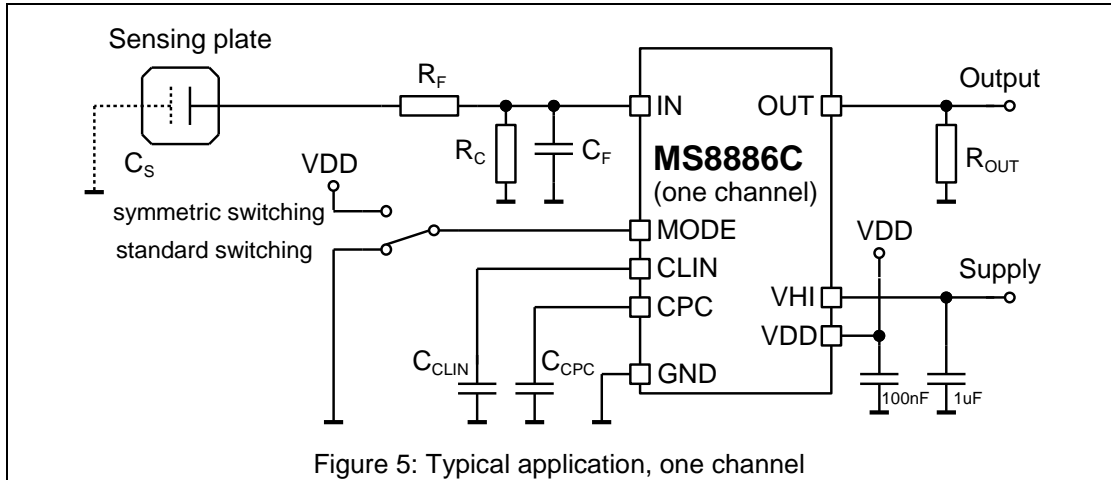


Figure 5: Typical application, one channel

The sampling rate is determined by the capacitance  $C_{CLIN}$  on pin CLIN. The rate can be adjusted from 300Hz to 3kHz. A 1kHz rate can be defined using  $C_{CLIN} = 22pF$ . A higher sampling rate reduces the reaction time and increases the current consumption.

The sensing plate capacitance  $C_S$  may consist of a small metal area, for example behind an isolating layer. The sensing plate is connected to a coaxial cable ( $C_{CABLE}$ ) which in turn is connected to the input pin IN. An internal low pass filter is used to reduce RF interference. An additional low pass filter consisting of a resistor  $R_F$  and capacitor  $C_F$  can be added to the input to further improve RF immunity as required. Typical values are  $R_F = 6.8k\Omega$  and  $C_F = 10pF$ . For good performance, the total amount of capacitance on the input ( $C_S + C_{CABLE} + C_F$ ) should be in the range 10pF to 60pF, the optimum point being around 30pF. These conditions allow the control loop to adapt to the static capacitance on  $C_S$  and to compensate for slow changes in the sensing plate capacitance. A higher capacitive input loading is possible (maximum 200pF) provided that an additional discharge resistor  $R_C$  is placed as shown in Figure 2. Resistor  $R_C$  simply reduces the discharge time such that the internal timing requirements are fulfilled. A typical value for  $R_C$  is between 5 and 50k $\Omega$ .

The sensitivity of the sensor can be influenced by the sensing plate area and capacitor  $C_{CPC}$ . Typically  $C_{CPC}$  is 470nF. The sensitivity is significantly reduced when  $C_{CPC} = 100nF$ . Maximum sensitivity is reached when  $C_{CPC} = 2.2\mu F$  but this also increases sensitivity to interference. The CPC pin has high impedance and is sensitive to leakage currents. Therefore  $C_{CPC}$  should be a high quality foil or ceramic capacitor, for example an X7R type.

**9.3 Switching dynamic selection**

Two different switching dynamics can be selected using the pins MODE[1:2]. For most applications the standard asymmetric switching behaviour is recommended. For proximity sensing applications with high sensitivity setting, it can be beneficial to use the symmetric switching behaviour.

- The standard switching mode (MODE pin connected to GND) implements an *asymmetry* between on-switching and off-switching requirements. For on-switching a relatively larger input capacitance increase is required, than the input capacitance

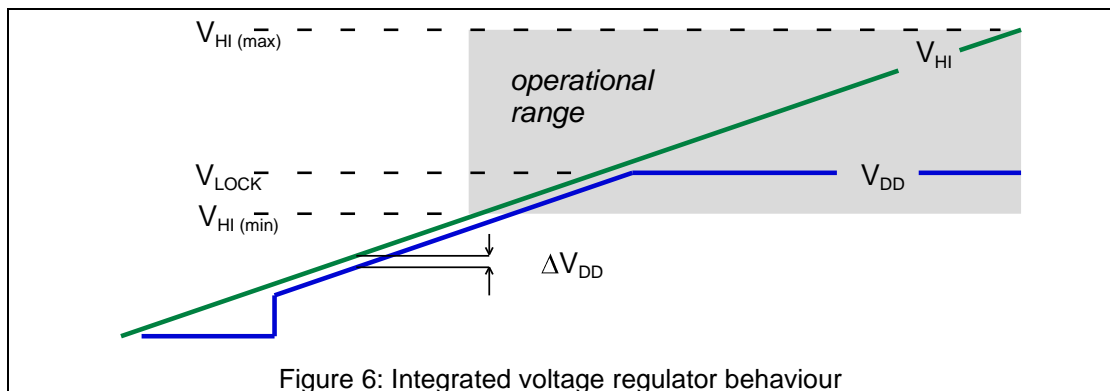
decrease required for off-switching. This implementation assures robust off-switching performance even under noisy environmental conditions.

- In the *symmetric* switching mode (MODE pin connected to VDD), the input capacitance change required for on-switching is similar to the capacitance change needed for off-switching. This mode supports proximity applications, where symmetrical on- and off-switching sensitivity is required to avoid unexpected behaviour.

Important: The switching dynamic can be set for each channel individually. When the symmetric switching mode is desired, the MODE pin has to be connected to the VDD pin of the **same** channel. The MODE pins **must not** be connected to the external supply voltage.

#### 9.4 Internal voltage regulator

The circuit has an integrated voltage regulator, supplied by pins  $V_{HI}[1:2]$ , that provides an internal  $V_{DD}$  supply, limited to a maximum of 4.6 V. The lock-in voltage,  $V_{LOCK}$ , on  $V_{HI}[1:2]$  is typically 4.0 V. The regulated supply is available at pins  $V_{DD}[1:2]$  and can be used to supply power to external electronic components (0.5mA maximum). Figure 6 shows the relationship between  $V_{HI}[1:2]$ ,  $V_{LOCK}$  and  $V_{DD}[1:2]$ .



The voltage regulators of the two channels are independent from each other, and the  $V_{DD}[1:2]$  voltages must therefore not be connected.

## 10 Electrical characteristics

### 10.1 Limiting values and ESD protection

Name	Parameter	Min	Max	Unit
$V_{HI}$	Positive supply wrt to GND[1:2]	-0.5	9.0	V
$V_{IN}$ , $V_{MODE}$ , $V_{CPC}$	Input voltage on pins IN[1:2], MODE[1:2], CPC[1:2]	-0.5	$V_{DD}+0.5$	V
$I_{OUT}$	Output current on pins OUT[1:2] to GND	-10	50	mA
$I_{GND}$	Total current to GND[1:2]	-10	50	mA
$I_{PIN}$	Current through any pin	-10	10	mA
$P_{TOT}$	Power dissipation		100	mW
$T_{stg}$	Storage temperature	-60	+125	°C
$V_{ESD}$	electrostatic discharge voltage		+/- 2000	V
	HBM		+/- 200	V
	MM			

### 10.2 DC Characteristics

Conditions:  $V_{HI} = 5V$  DC,  $T = 25^{\circ}C$ , if not stated otherwise

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{HI}$	Positive supply		2.7 <sup>2</sup>		9.0	V
$V_{LOCK}$	Regulator lock-in voltage	No external load		4.0		V
$V_{DD}$	Regulated internal supply	$V_{HI} > V_{LOCK}$	3.0	4.0	4.6	V
$V_{DD}$	Internal supply	VDD connected to VHI	2.7 <sup>3</sup>		4.6	V
$\Delta V_{DD}$	Regulator voltage drop	$V_{HI} < V_{LOCK}$ , no external load on $V_{DD}$		10	50	mV
$I_{HI}$	Operating current	Idle state <sup>3</sup> per channel, output inactive, $f_k = 1$ kHz		3	5	uA
		Idle state <sup>3</sup> per channel, output inactive, $f_k = 1$ kHz, $V_{HI} = 3.0V$		2.2	3.5	uA
$I_{SINK}$	Output sink current	Internal constant current to GND[1:2]		150		nA
$V_{IL}$	Input low level	MODE[1:2] pins	0.7 $V_{DD}$		$V_{DD}$	V
$V_{IH}$	Input high level	MODE[1:2] pins	$V_{SS}$		0.3 $V_{DD}$	V
$V_{OUT}$	Output voltage	OUT[1:2] pins	0	$V_{HI}$	9.0	V
$I_{OUT}$	Output current	Operating range of output stage <sup>4</sup>	0	10	20	mA
$V_{FOUT}$	Output saturation voltage	OUT[1:2] pins: $I_{OUT} = 10$ mA	0.1	0.2	0.4	V
		OUT[1:2] pins: $I_{OUT} = 10$ mA, $V_{HI} = 3.0V$	0.1	0.3	0.5	V
$C_{VDD}$	Ext. $V_{DD}$ decoupling capacitor	Ceramic chip capacitor recommended on VDD[1:2]	100		220	nF
$V_{CPC}$	Reservoir capacitor voltage	Usable control range on pins CPC[1:2]	0.6		$V_{DD}-0.3$	V
$I_{L,CPC}$	Reservoir capacitor leakage current	Low leakage X7R ceramic type recommended			1	nA
$T_{amb}$	Operating temperature range		-40	25	85	°C

<sup>2</sup> When the input capacitance range is limited to  $10pF \leq C_{IN} \leq 40pF$ , or an external pull down resistor  $R_C$  is used, the device can be operated down to  $V_{HI}=3.0V$  over the full temperature range.

When the input capacitance range is limited to  $10pF \leq C_{IN} \leq 30pF$  or an external pull down resistor  $R_C$  is used, the device can be operated down to  $V_{IH}=2.7V$  over the reduced temperature range  $0...70^{\circ}C$ .

<sup>3</sup> Idle state is the steady state after completed power-up, without any activity on the sensor plate, and the voltage on the reservoir capacitor  $C_{CPC}$  settled.

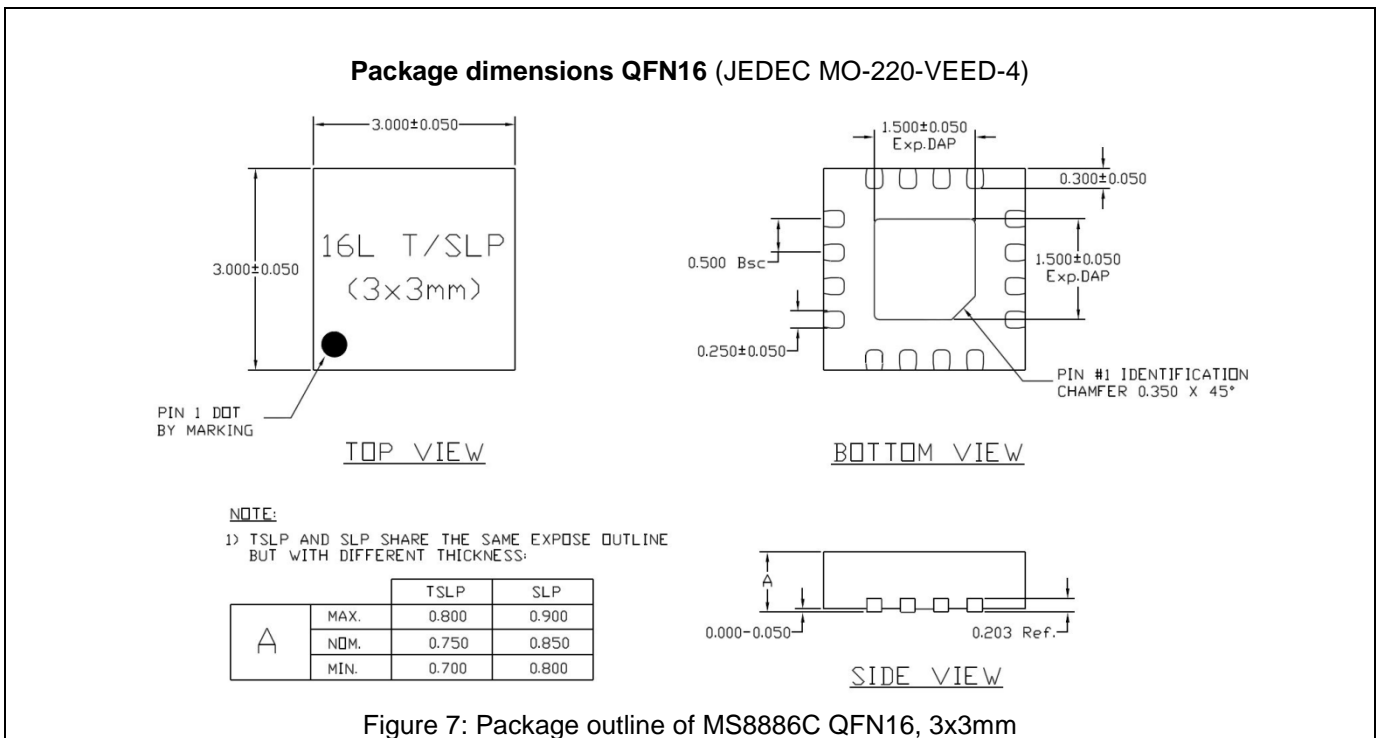
<sup>4</sup> For reliability reasons the average output current must be limited to maximum  $4.6mA@70^{\circ}C$  and  $3.0mA@85^{\circ}C$

## 10.3 AC Characteristics

Conditions:  $V_{HI} = 5V$  DC,  $C_{CLIN} = 22pF$ ,  $C_{CPC} = 220nF$ ,  $T = 25^{\circ}C$ , if not stated otherwise

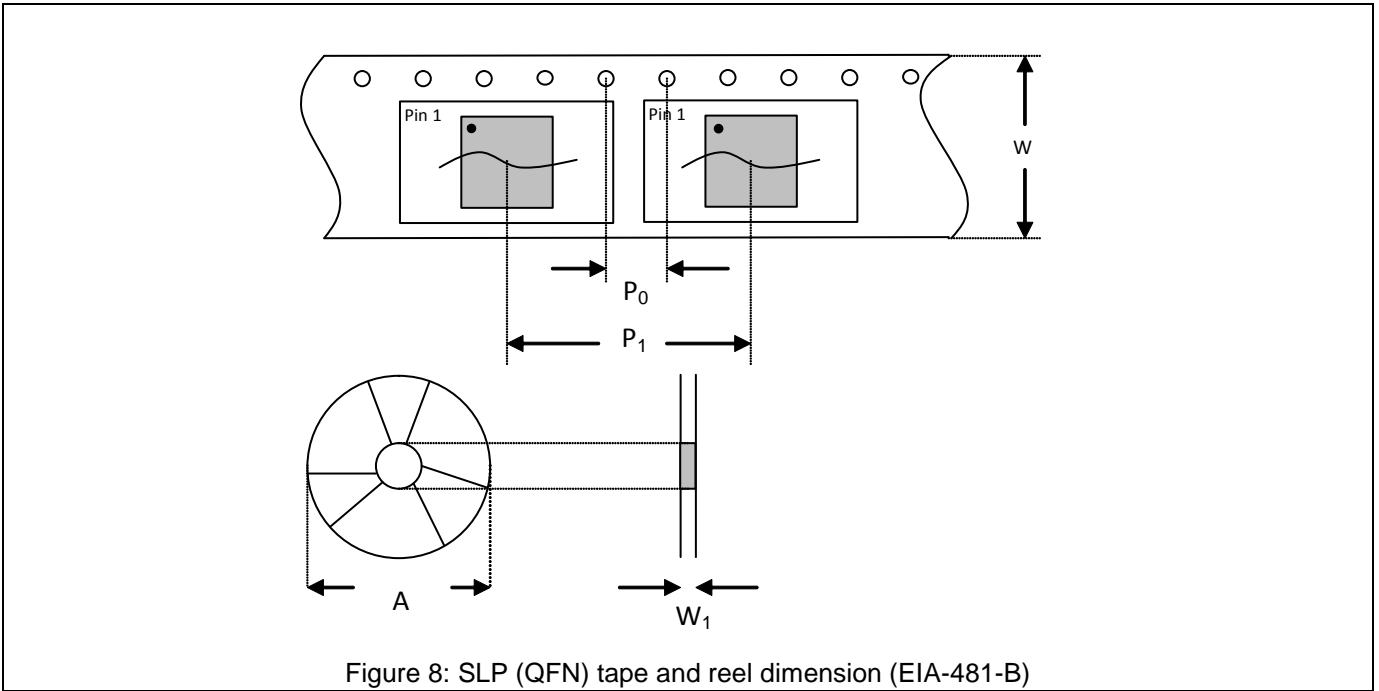
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{CLIN}$	Oscillator capacitance	Operating range	0	22	100	pF
$C_{CPC}$	Reservoir capacitor	Low leakage X7R ceramic type recommended	47	220	2500	nF
$C_{IN}$	Input capacitance	Sensing plate + parasitic	10		60	pF
		Sensing plate + parasitic, $V_{HI}=3.0V$ , full temperature range	10		40	pF
		Sensing plate + parasitic, $V_{HI}=2.7V$ , over the reduced temperature range 0...70°C.	10		30	pF
$t_{WAIT}$	Power-on start-up time	Until idle state is established		0.5		s
$f_K$	Sampling rate	$C_{CLIN} = 0$		3.3		kHz
		$C_{CLIN} = 22 pF$		1		kHz
		$C_{CLIN} = 100 pF$		275		Hz
$t_{SW}$	Reaction time on sensor capacitance change	$f_K = 1 kHz$ , MODE[1:2] connected to GND[1:2]		64		ms
		$f_K = 1 kHz$ , MODE[1:2] connected to VDD[1:2]		32		ms

## 11 Package outlines



**12 Tape and reel specification**

Item	Parameter	Tape Type Size 12mm
1	Pin1 Orientation	As given in Figure 8.
2	Hole pitch P0 (see Figure 8)	4mm
3	Pocket pitch P1	8mm
4	Tape width W (see Figure 8)	12mm
5	Material base tape	Polystyrene (PS+C)
6	Material top cover	Antistatic Polyester Film
7	Reel hub width W1 (see Figure 8)	12 mm
8	Reel diameter A (see Figure 8)	330mm



**13 Legal disclaimer**

This product is not designed for use in life support appliances or systems where malfunction of these parts can reasonably be expected to result in personal injury. Customers using or selling this product for use in such appliances do so at their own risk and agree to fully indemnify Microdul AG for any damages resulting from such applications.

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